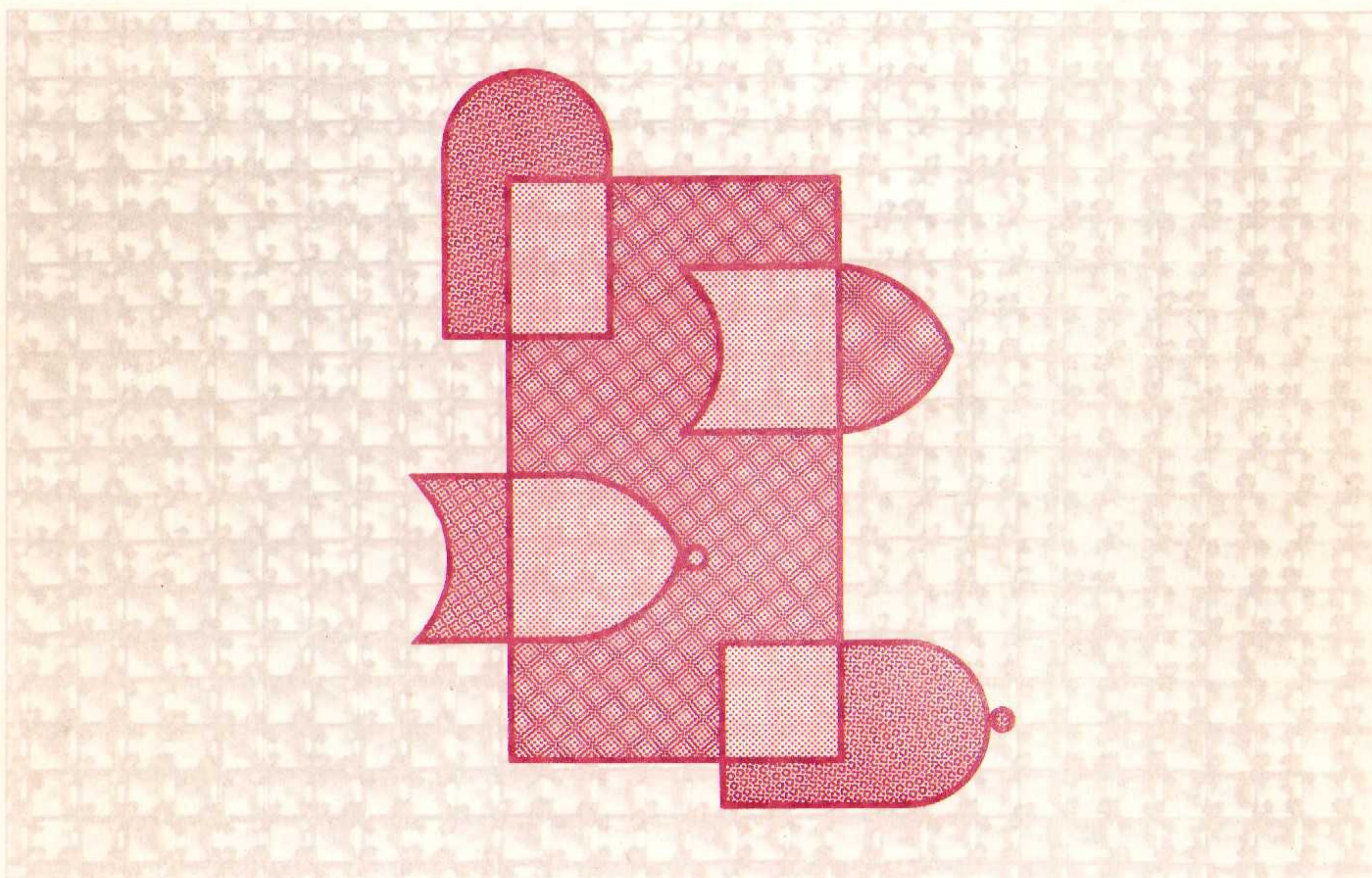


TECHNISCHE DOCUMENTATIE 1970

DEEL 1 2 3 4 5 6 7 8 9 10 11 12

TECHNISCHE GEGEVENS TTL



VOIN OLOIN
ELEKTRONICA

Snellemanstraat 10-11 bij Zwaanshals, Rotterdam - noord
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Giro: 29 55 50. Bankrelatie: Amsterdam-Rotterdam Bank NV.
Postorders en correspondentie: Postbus 3149 te Rotterdam

Filiaal: Blasiusstraat 14-16 bij Ceintuurbaan, Amsterdam
Telefoon: 020-947218.

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Verhuizingen van abonné's.

Elke abonné is in ons adresseersysteem ondergebracht onder een op de enveloppe vermeld administratienummer. Bij verhuizing, adrescorrectie of correspondentie over Uw abonnement dient beslist dit nummer te worden vermeld. Correspondentie dient U uitsluitend te richten aan: Van Dam Elektronica, Afd. TD 1970, Postbus 3149, Rotterdam.

Inleiding.

Coördinatie: Paul E. Annokkee

Deze nieuwe uitgave in 1970 wordt geheel in beslag genomen door een steeds verder in de belangstelling komende reeks produkten, namelijk:

TTL digitale geïntegreerde schakelingen en aanverwante produkten.

In deze documentatie wordt op een uitgebreide manier ingegaan op de technische gegevens van 29 TTL IC's, terwijl een speciaal gedeelte gereserveerd is voor de meetschakelingen, waarmee desgewenst de betrokken specificaties kunnen worden gecontroleerd.

De in deze documentatie besproken geïntegreerde schakelingen zijn uit voorraad magazijn Rotterdam leverbaar. Het TTL programma wordt maandelijks uitgebreid met één of meerdere nieuwe typen (binnenkort o.a. ook up-down decade counters, arithmetic logic unit and function generators, dual one shot multivibrator); in een latere uitgave worden de nieuwe typen in totaliteit opgenomen.

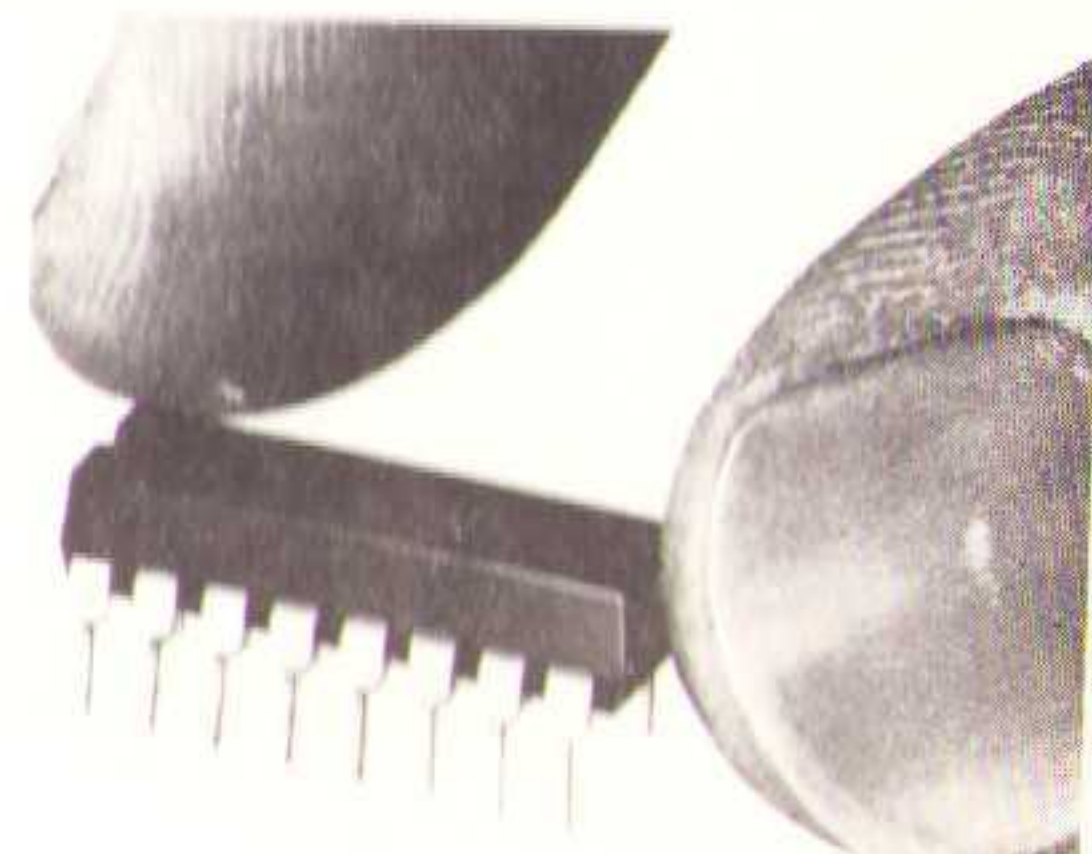
Wij wijzen U gaarne op de in de prijslijst opgenomen staffelprijs-notering. Deze is van toepassing voor het totale aantal bestelde geïntegreerde schakelingen, ongeacht de bestelde typen en het aantal per type. In verband met mogelijke prijswijzigingen is deze prijslijst los uitgevoerd.

Op pagina 68 hebben wij een overzicht opgenomen van volkomen uitwisselbare typen TTL IC's van fabrikanten als Texas Instruments, National Semiconductor, AEG, Amperex, ITT, Fairchild, Ferranti, Motorola, Sescosem, Transitron, Sprague, Siemens, SGS en Signetics. Zoals uit deze lijst valt af te leiden, is in het typenummer van de meeste fabrikanten de code 7400 verwerkt, zodat een snelle herkenning mogelijk is geworden.

Tot slot wijzen wij U nog op de op pagina 3 opgenomen gebruiksaanwijzingen van de besproken produkten. Teneinde de gewenste resultaten te kunnen bereiken is het in acht nemen van de besproken punten van groot belang.

van dam
ELEKTRONICA

voor levering uit voorraad
van produkten, die bewijzen
dat de vooruitgang in de
techniek nog steeds doorgaat.



Here are helpful general rules-of-thumb regarding practical uses of standard TTL Series 54/74.

GENERAL	GATES	LINE DRIVING AND RECEIVING	
<u>Power supply</u> Maintain ripple $\leq 5\%$. Maintain regulation $\leq 5\%$. R-F bypass supply primary. <u>Decoupling</u> Decouple every 5 to 10 packages with r-f capacitors of 0.01 to 0.1 μF. <u>Grounding</u> A ground plane is desirable, especially when the p-c board contains a large number of packages. If no ground plane is used, incorporate ground bus around p-c board periphery where possible. Make ground bus as wide as possible. Always return both ends of long ground bus to common point (system ground). <u>Flip flops</u> <u>Preset and clear pulses</u> If clock pulse is present, maintain preset or clear pulse until clock pulse goes low. <u>Clock pulse</u> Rise and fall times should be less than 150 ns to improve noise immunity. <u>Input data</u> In general, input data of master slave J-K flip flops should be held constant from the leading edge of the clock pulse until 5 ns before the negative going edge of the clock pulse. The D type flip flop has a setup and hold time centered around the positive edge of the clock which must be observed.	<u>Data input rise and fall times</u> Reduce as driver output impedance increases. Should be no greater than 1 μs for Z. ≥ 100 ohms. <u>Data pulse width</u> Maintain above 25 ns. <u>Unused inputs of AND and NAND gates and unused preset, and clear inputs of flip-flops</u> Tie directly to V_{CC} where V_{CC} is guaranteed to always be $\leq 5.5\text{V}$; or Tie to V_{CC} through resistor $\geq 1\text{K}$ ohms. Several unused inputs can be tied to one resistor; or Tie to used input of same gate if maximum fan-out of driving device will not be exceeded; or Tie to unused gate output where unused gate input is grounded. <u>Unused inputs of NOR gates</u> Tie to ground. <u>Unused gates</u> Tie inputs of unused gates to ground for lowest power drain. <u>Increasing gate/buffer fan-out</u> Parallel gates/buffers of same package. <u>Expanders</u> Place expanders as close as possible to the gate being expanded and avoid capacitance loading of the expander nodes to minimize degradation of switching speeds. Switching speed degrades approximately 1.1 ns for each pF of capacitance at the expander nodes.	<u>Single-wire interconnections</u> May be used up to approximately 10 inches without particular precaution. A ground plane is always desirable. If longer than 10 inches, ground plane is mandatory with wire routed as close to it as possible. Use twisted pair of coax lengths exceeding 20 inches. <u>Coaxial and twisted pair cables</u> Design around a pair of approximately 100 ohms characteristic impedance. Higher impedances increase crosstalk while lower impedances are difficult to drive. a. coaxial cable of 93 ohms impedance (such as Micro-dot 293-3913) is recommended; b. for twisted pair Nos. 26 or 28 wire with thin insulation twisted about 30 turns/foot work well. <u>Transmission-line ground</u> Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. <u>Resistive pull-up</u> Use 500 to 1,000 ohms resistive pull-up at receiving end of long cables for added noise margin and more rapid rise times. <u>Line termination</u> Reverse terminate with 27 to 47 ohms at driving end in series with the line to prevent negative overshoot.	<u>Gates as line drivers</u> Drive into only one transmission-line terminated with one gate input. Adverse effects from multiple loads include: a. erroneous signals due to line reflection; b. long delay times; c. excessive driver loading. <u>Gates as line receivers</u> Use only one gate input to terminate line. Follow unused input rules for receiver gates. <u>Flip flops as line drivers</u> Generally unsatisfactory due to the possibility of collector commutation from reflected signals. <u>Decoupling</u> Always decouple driving/receiving devices in addition to normal decoupling. Use 0.1 μF r-f capacitors located at V_{CC} and ground pins. <u>Long lines</u> For driving long lines and for sending data in the most reliable way the line driver and line receiver combination should be used. In this way, differential signals can be sent and the response of the receiver shaped so as to optimize speed or high frequency rejection.

NOISE IN 54/74 TTL SYSTEMS

by
Bill Heniford

Few subjects are so inclusive in scope and varied in connotation as the generalized term "noise." Noise may be loosely defined as undesired signals, whether sonic, magnetic, electric, or any number of others. The major area of interest here will be extraneous voltages and currents in digital logic systems and specifically Texas Instruments SN5400/SN7400 TTL systems.

Figure 1a is a typical digital logic circuit. The effects of noise coupled into the circuit can be seen in Figure 1b and 1c. In Figure 1b a small noise pulse is present on the clock line, but the flip-flop does not respond as it does to the greater pulse in Figure 1c.

If this circuit were part of some arbitrary decision-making system, the conditions in Figure 1c would produce erroneous answers — usually worse than no answer at all. The noise present in Figure 1b, while undesirable, is not really harmful.

The origins and characteristics of such noise will be considered along with device characteristics pertinent to the subject. Methods will then be investigated to eliminate or counteract the effects of noise in logic systems. Full use will be made of the superior characteristics of SN5400/SN7400 TTL devices.

NOISE TYPES AND CONTROL METHODS

Several types of noise must be dealt with in logic systems. The following classifications of noise will be used as defined:

1. External noise — environmental noise radiated into the system. Such noise results from circuit breakers, brush motors, arcing relay contacts, or magnetic field generating activity.
2. Power line noise — noise coupled through the a-c or d-c power distribution system. Initial sources are frequently the same as those of external noise.
3. Crosstalk — noise induced into signal lines from adjacent signal lines.
4. Signal current noise — noise generated in stray impedances throughout the circuit from the flow of required signal currents.
5. Transmission line reflections — unterminated transmission lines cause ringing and overshoot.

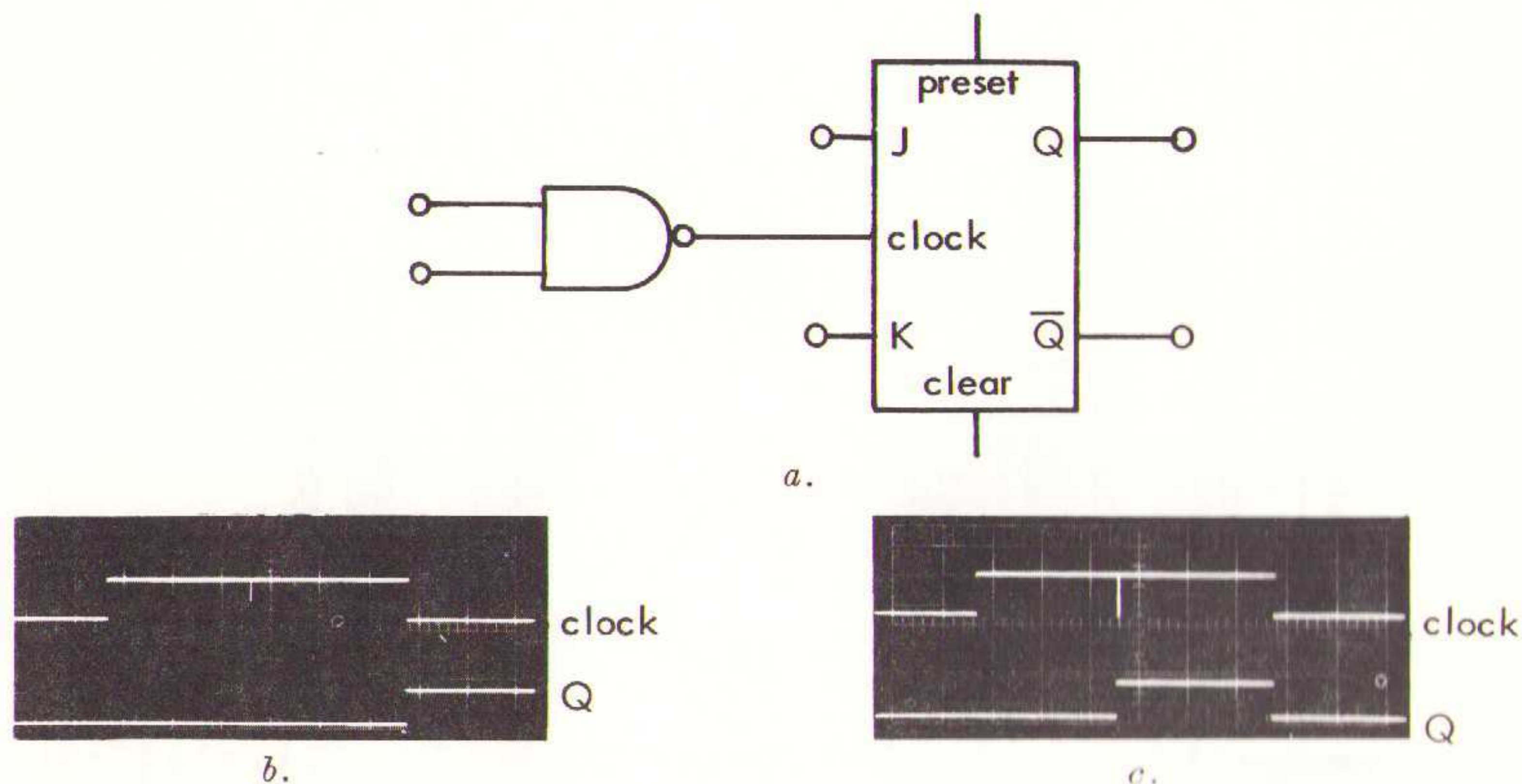
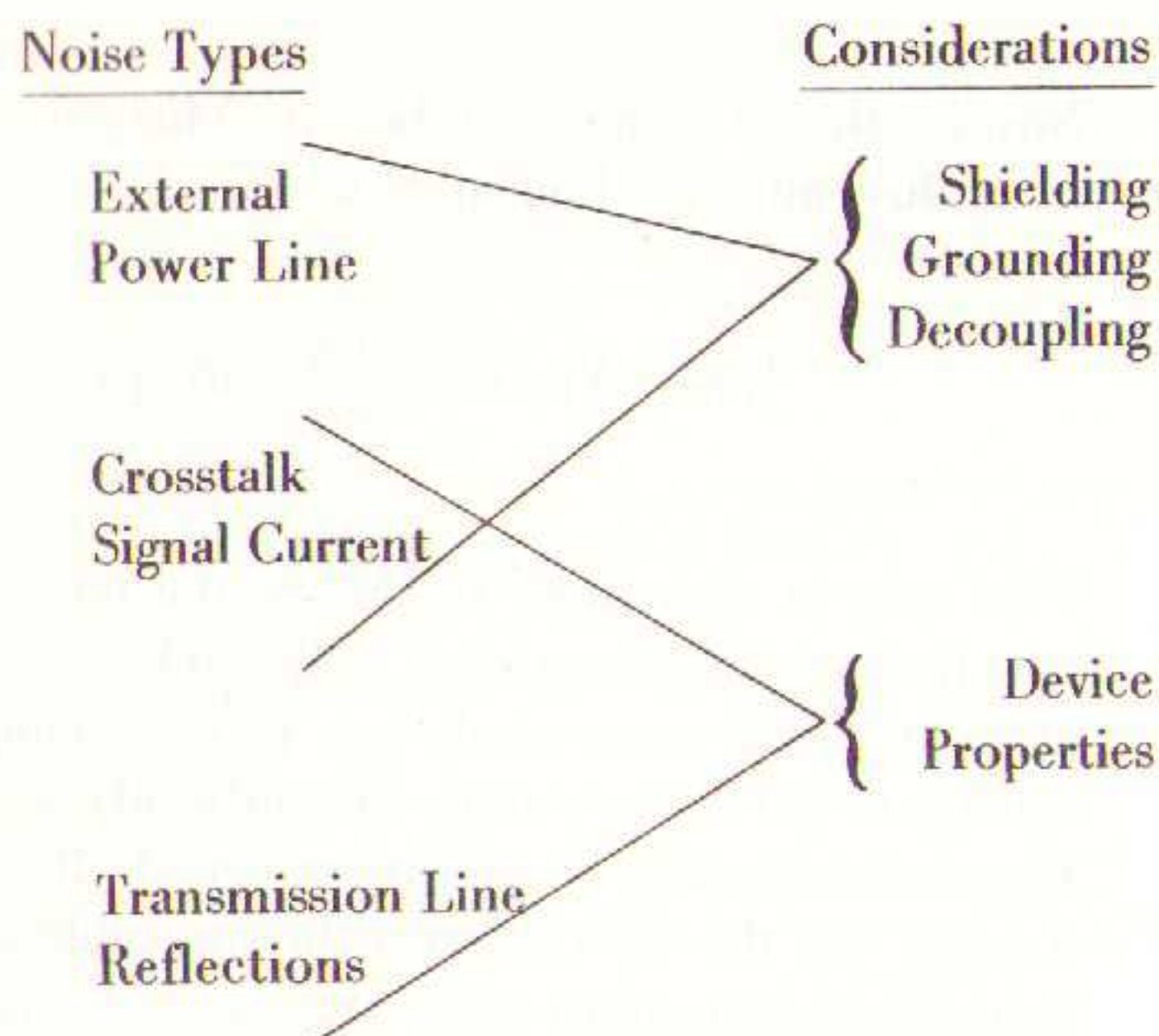


FIGURE 1. Typical Logic Circuit With Noisy Inputs

In general, noise categories defined above may be dealt with according to the following:



These noise fields are usually changing at a rapid rate; thus, the aperture required to exclude them may be quite small. For effective exclusion, the sensitive circuitry must be completely shielded. While aluminum or similar materials may be effective in stopping electrostatic noise, only a ferrous metal can successfully protect equipment against magnetic fields. It is helpful to connect the system to a good earth ground; but the shield system must be complete and must be grounded to the system ground; otherwise the shield may couple the noise on into the system.

External noise may be conducted into the system from the power lines. Decoupling and filtering of these lines should be standard design procedure.

Fast systems of logic are generally assumed to be more susceptible to externally generated noise than are slower systems due to the greater bandwidth. This assumption contains some truth, but it is not as relevant as is widely held. A slow logic system is less susceptible to noise than a faster one only if it is slow compared with the noise signals. One of the fastest of the industrial noise generators is the silicon controlled rectifier (SCR, Thyristor, etc.). These devices produce rise-times of about 1 microsecond. Edges as fast as this are slow when compared with even the slowest types of integrated circuit logic elements. For example, MOS

SHIELDING

Electrical equipment must function in an extremely noisy environment exclusive of its own internally generated noise. Noise pulses may come from many sources, but will be either an electrostatic field or electro-magnetic field or both. The noise wavefront must be prevented from entering the equipment.

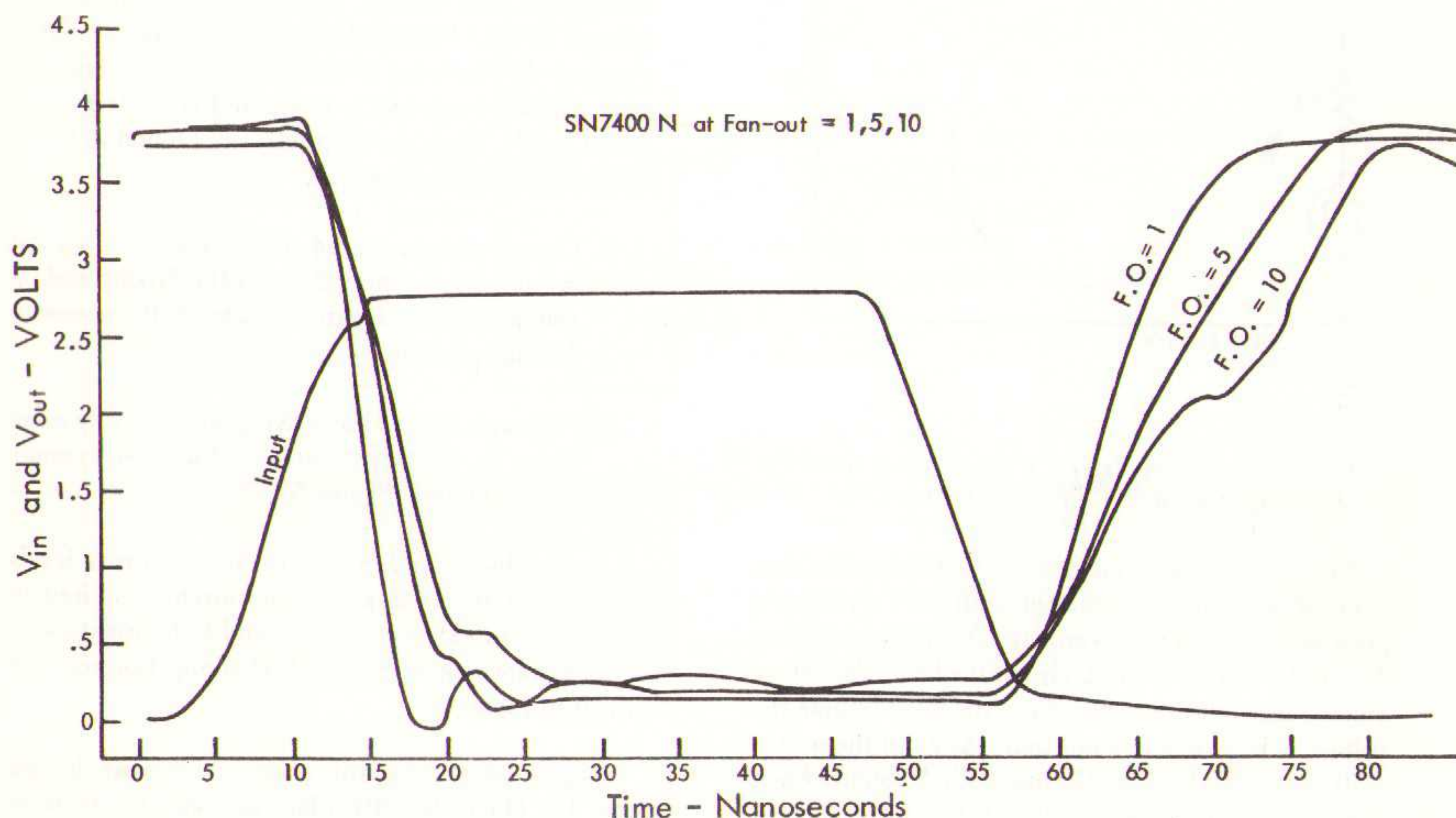


FIGURE 2. Typical SN5400/7400 Switching Times at 25°C

is probably the slowest I/C logic, yet it has propagation delay of about .5 microsecond and is as susceptible to industrial noise as is the fastest TTL. Actually, TTL has such low impedance that it is less susceptible to noise than MOS or any other logic system.

GROUNDING AND DECOUPLING

In the generation of internal noise the total propagation delay is of secondary importance; it is the actual transition time that determines the amplitude/frequency spectrum of the generated signal at the higher harmonics. See Figure 2. Application of the Fourier Integral to these SN5400/SN7400 series waveforms shows frequency components of significant amplitude exceeding 100 megahertz. In consideration of the frequency spectrum generated when an SN5400/SN7400 device switches, it is obvious that a system using these devices must receive consideration from an RF viewpoint if trouble is to be avoided, even though the repetition rates may be only a few hertz. The transient currents generated by capacitance charging, changes in levels of direct currents, line driving, etc., must be considered. For example, a gate driving a transmission line may be represented by a voltage source E having an output impedance Z_s connected to an impedance Z_o , and loaded with resistance R . See Figure 3.

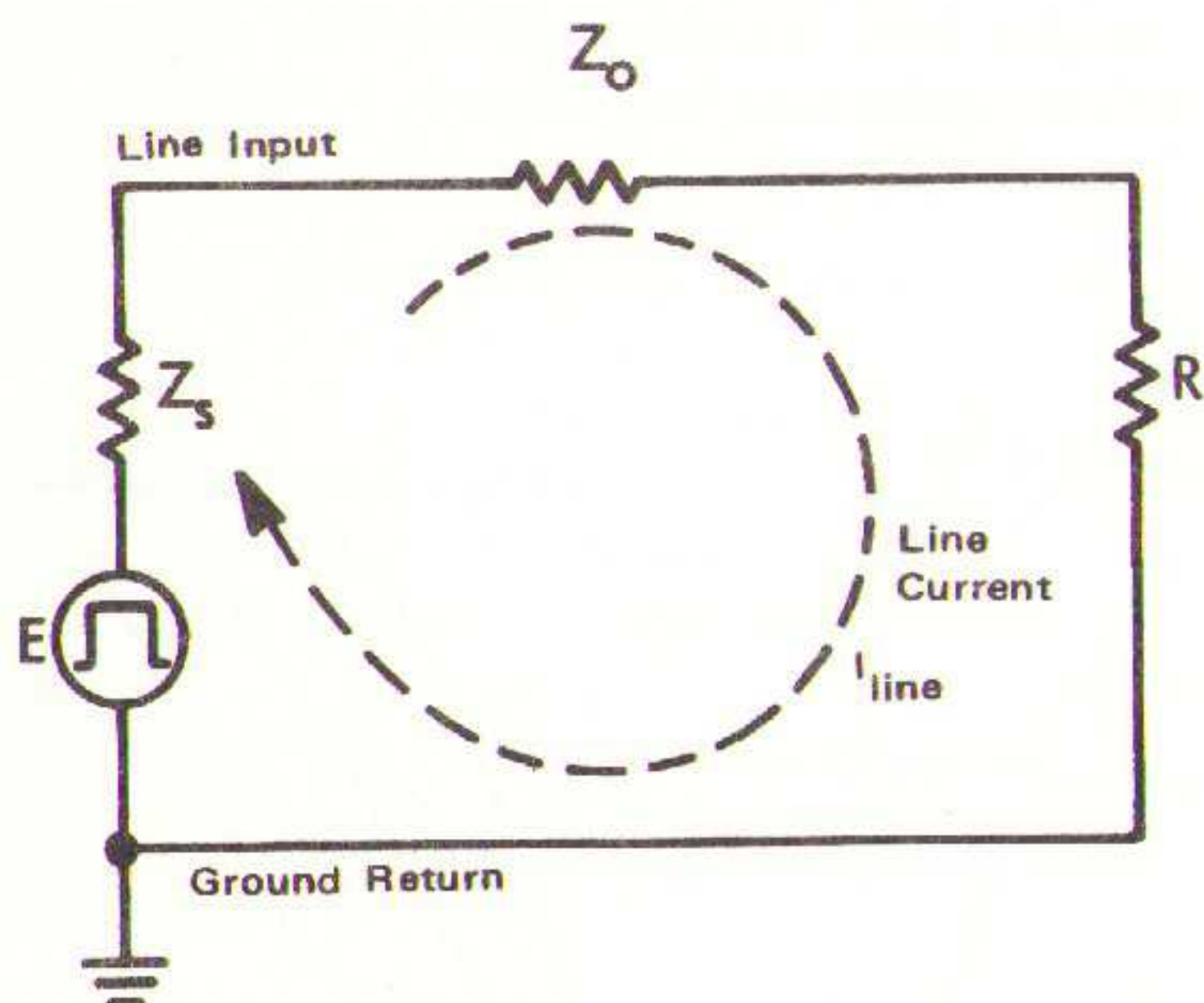


FIGURE 3. Simplified Circuit of a Gate Driving a Loaded Transmission Line

From transmission line theory (1), line termination is not a factor in drive current until after a reflected pulse returns from the termination to the transmitting device. In a practical TTL circuit the line termination must be high relative to the Z_o of the line. Assume the voltage E is 5 volts in amplitude, the Z_s of the source is 50 ohms, and the Z_o of the line is also 50 ohms. When E makes the transition from 0 volts to 5 volts, the vol-

tage across the input of the line will be, by Ohm's law,

$$V_{in} = E \frac{Z_o}{Z_s + Z_o} = 2.5 \text{ volts}$$

Now for the 50 ohm line to become charged, a current must flow onto the line equal to:

$$I_{line} = V_{in}/Z_o = \frac{2.5}{50} = 50 \text{ mA}$$

This current also flows in the ground return, in this case the twisted pair ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the currents flowing see the discontinuity in the cable as a high impedance, and a noise spike is generated. Viewed in a slightly different manner, the ground current sees a low impedance and a current cancellation if the ground is properly carried through; if not, it sees a high impedance. See Figure 4 for a specific example. Assume the gate driving the line is switched from the "1" to the "0" state. Current flows as indicated by the arrow marked I . Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate #3. If the ground return is properly made, desirable results are obtained in that the impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two rules to reduce transmission line current effects to acceptable levels in TTL systems may be set forth. These are empirical rules found to be effective (see Figures 4 and 5):

1. Carry twisted pair and coaxial returns to a good ground termination close to the driving and receiving devices. Figure 4 illustrates the necessity for this practice.
2. Decouple V_{cc} of line driving and receiving gates close to the device with a .1- μ F disc ceramic capacitor (see Figure 5).

As the logic devices change state, current levels change due to different device currents required in each state, to external loading, and to transients such as capacitance charging and discharging. Consider the circuit in Figure 6.

As gate G1 switches off, its internal current changes from $I_{cc}(1)$ to $I_{cc}(0)$. Likewise gates G2 through

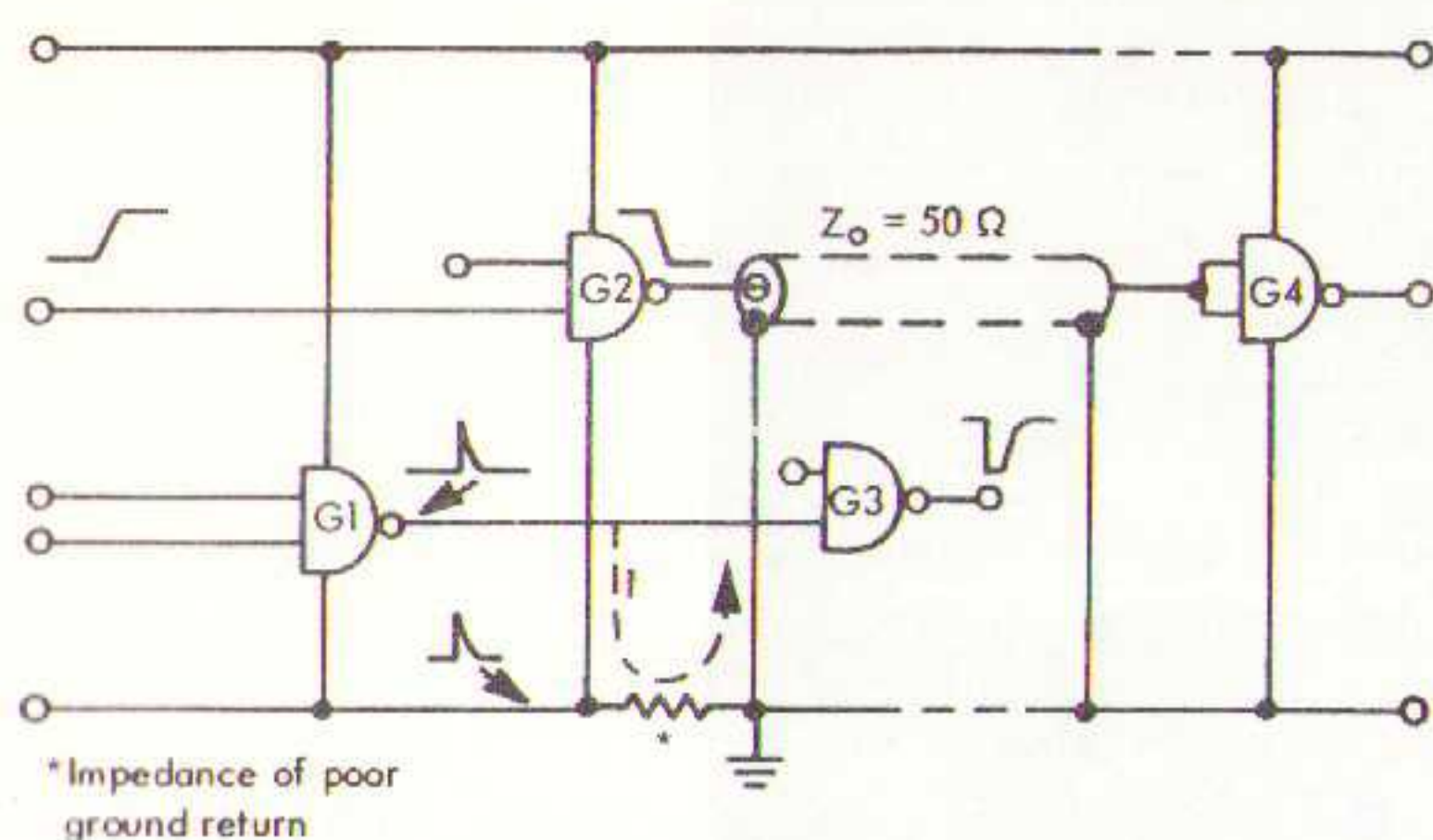


FIGURE 4. Noise Generation due to poor transmission line returns

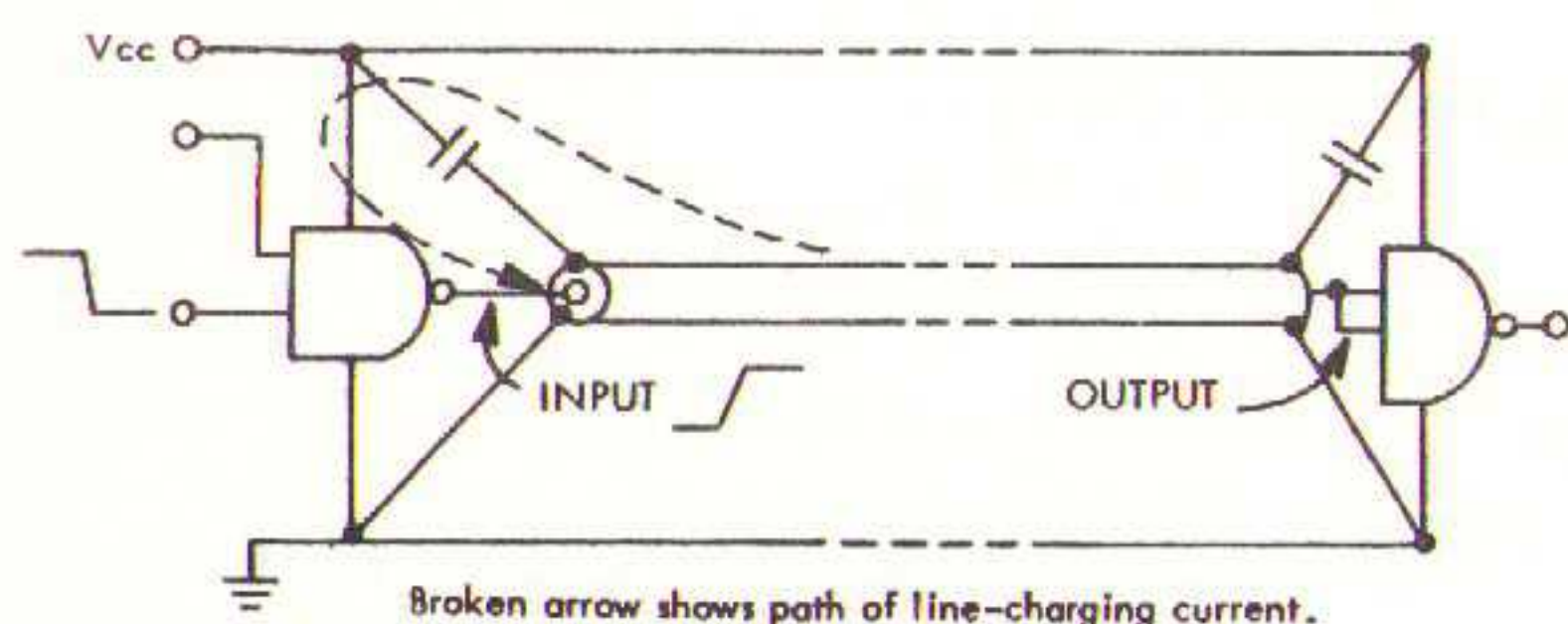


FIGURE 5. Ideal Transmission Line Current-Handling

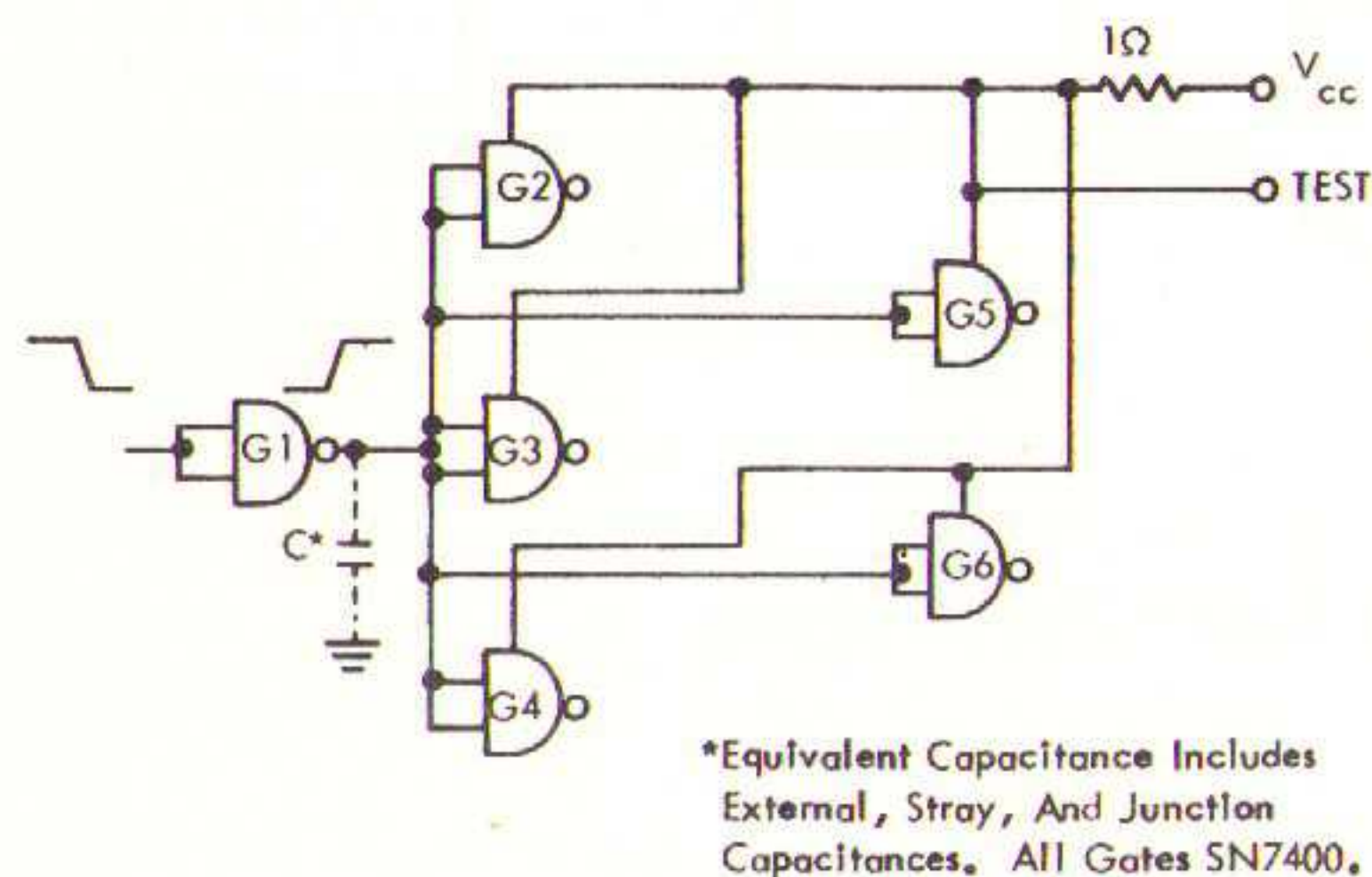


FIGURE 6. Test Circuit for I_{cc} Variation

G6 change from $I_{cc}(0)$ to $I_{cc}(1)$. Also C must be charged by a current:

$$I_c = C \, dV/dt$$

where C is 49 pF, and dV/dt is the output voltage swing divided by the output rise time. Taking the following typical data sheet parameters: (2)

$$I_{cc}(0) = 3 \text{ mA}$$

$$I_{cc}(1) = 1 \text{ mA}$$

$$t_r \approx 10 \text{ ns}$$

$$t_f \approx 5 \text{ ns}$$

working with these values:

$$\begin{aligned} \Delta I_{cc}(\text{DC}) &= [\text{no. of gates } (0 \rightarrow 1)] [I_{cc}(0) - I_{cc}(1)] \\ &\quad + [\text{no. of gates } (1 \rightarrow 0)] [I_{cc}(1) - I_{cc}(0)] \\ &= 1 [1 - 3] + 5 [3 - 1] \\ &= -2 \text{ mA} + 10 \text{ mA} \\ &= +8 \text{ mA} \end{aligned}$$

and

$$\begin{aligned} I_{cc}(\text{AC}) &= C \, dV/dt \\ &= (49 \times 10^{-12}) \left(\frac{4 \text{ V}}{10 \text{ ns}} \right) \\ &= (49 \times 10^{-12}) (4 \times 10^9) \\ &= 19.6 \text{ mA} \end{aligned}$$

Plotting these values gives the change in I_{cc} shown in Figure 7a. Actual observed values (Figure 7b) were as follows:

$$I_{cc}(\text{DC}) = +8 \text{ mA}$$

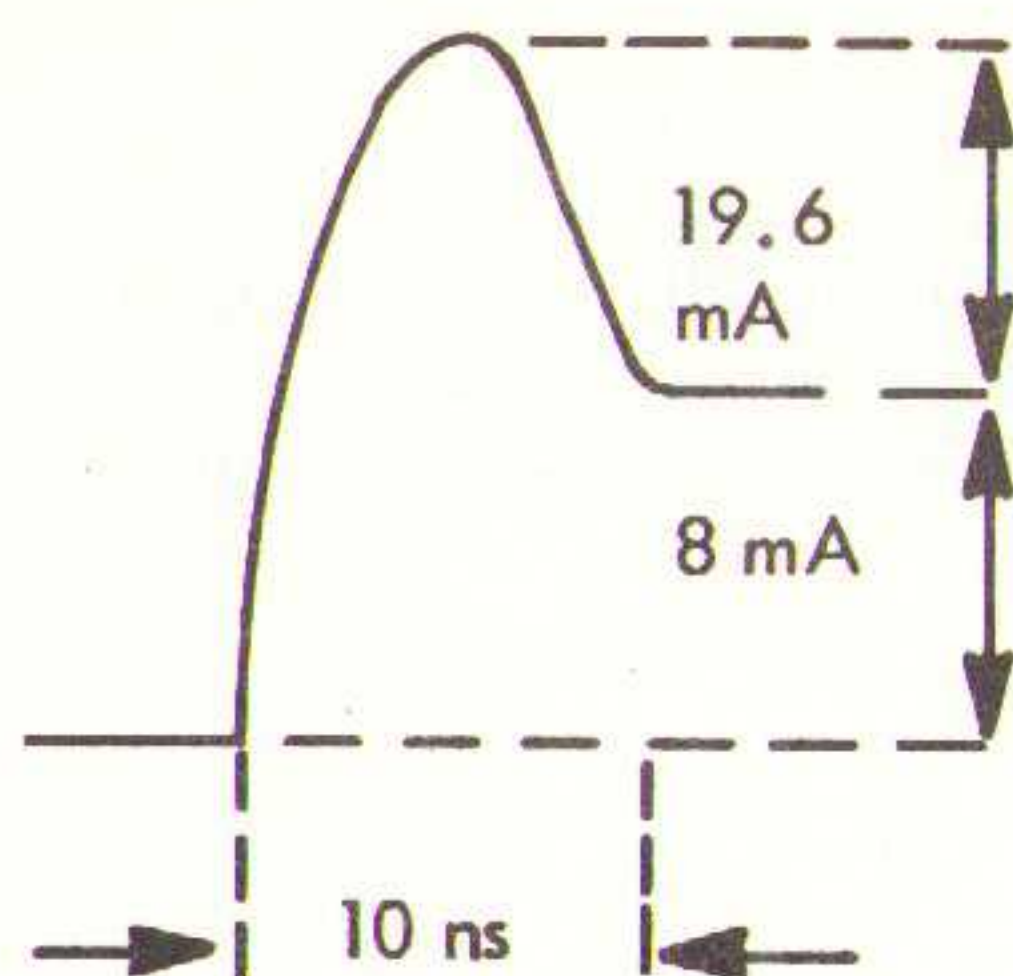
$$I_{cc}(\text{AC}) = +24 \text{ mA}$$

If gate G1 is now forced to switch to the "0" state, the ΔI_{cc} will reverse from the above figures; that is, it will increase by eight milliamperes. The transient, or a-c current is another matter however. As gate G1 turns off, it must discharge the capacitor C in Figure 6 through the R_{cs} of the output transistor to ground. Again, this current can be calculated from the voltage, capacitance and fall time of the output:

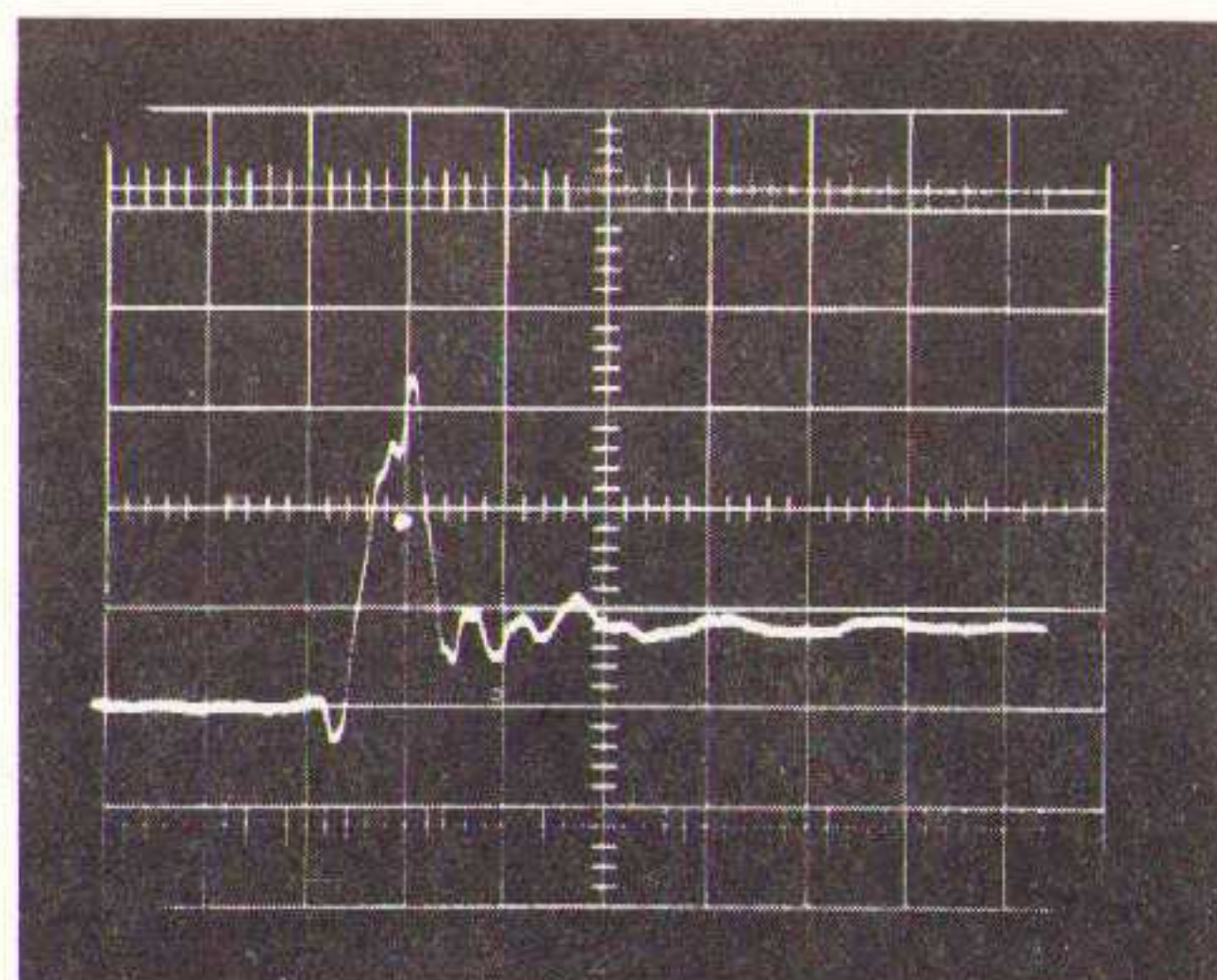
$$\begin{aligned} I_{\text{gnd}} &= C \, dv/dt = (49 \times 10^{-12} \text{ F}) (4 \text{ V}) / (5 \times 10^{-9} \text{ s}) \\ &= 39.2 \text{ mA} \end{aligned}$$

Since C is being discharged to ground, no transient current should be dumped onto the V_{cc} line. Tests have shown this to be true. This fact, plus the close agreement of the calculated and observed currents to charge capacitance C, should eliminate concern over the possibility of both output transistors having overlapping conduction times.

The flow paths of these currents have been investigated in order to intelligently explore the grounding



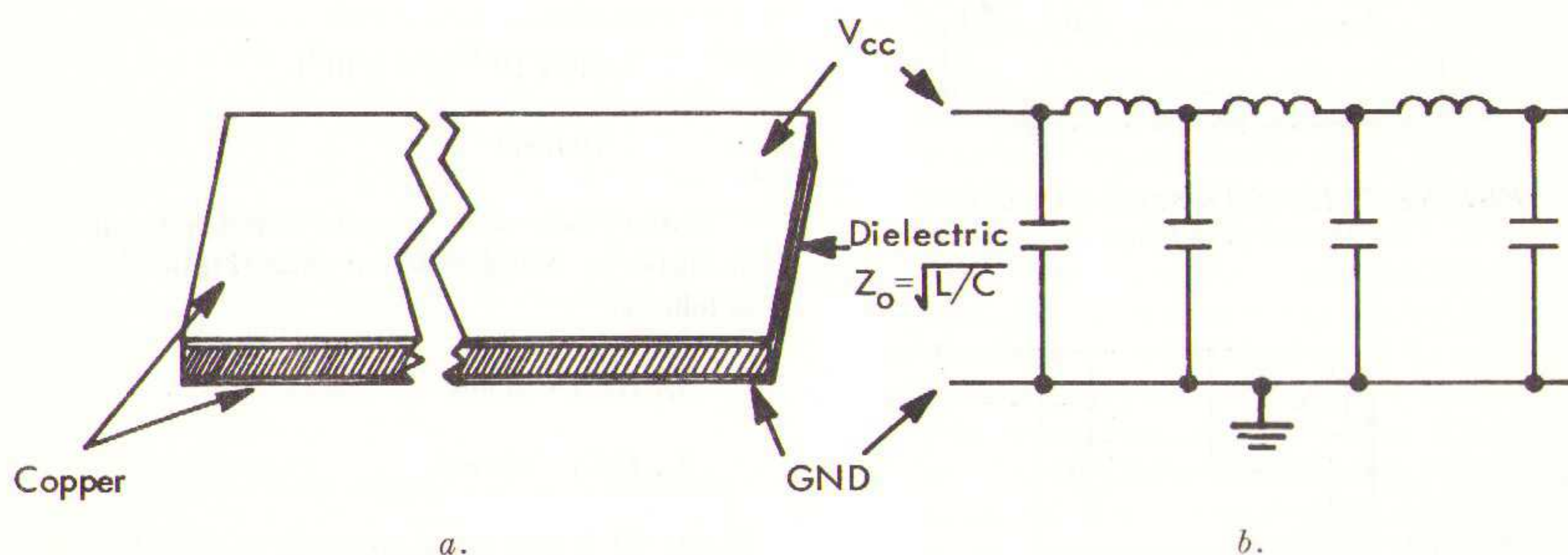
a.



Vert: 10 mA/cm
Horiz: 10 ns/cm

b.

FIGURE 7. I_{CC} Waveform From Figure 6 Circuit



a.

b.

FIGURE 8. "Transmission Line" Power Buses

and decoupling necessary to counteract their effects. V_{CC} decoupling thus may be approached in two ways; common to both is the requirement to maintain low impedance from the individual circuit V_{CC} to ground. First, the V_{CC} line may be considered a transmission line back to a low impedance supply. The positive bus may be laminated with a ground bus to form a strip transmission line of extremely low impedance as is done in some emitter-coupled logic systems (Figure 8a). Such a line may be electrically approximated with lumped capacitances (Figure 8b). The inductances in Figure 8b are usually a distributed component which must be minimized to lower the Z_0 of the line. An alternate approach is to consider the V_{CC} bus as a d-c connecting element only and provide a low-impedance path near the devices for the transient currents to ground (Figure 9). For effective filtering and decou-

pling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is one of

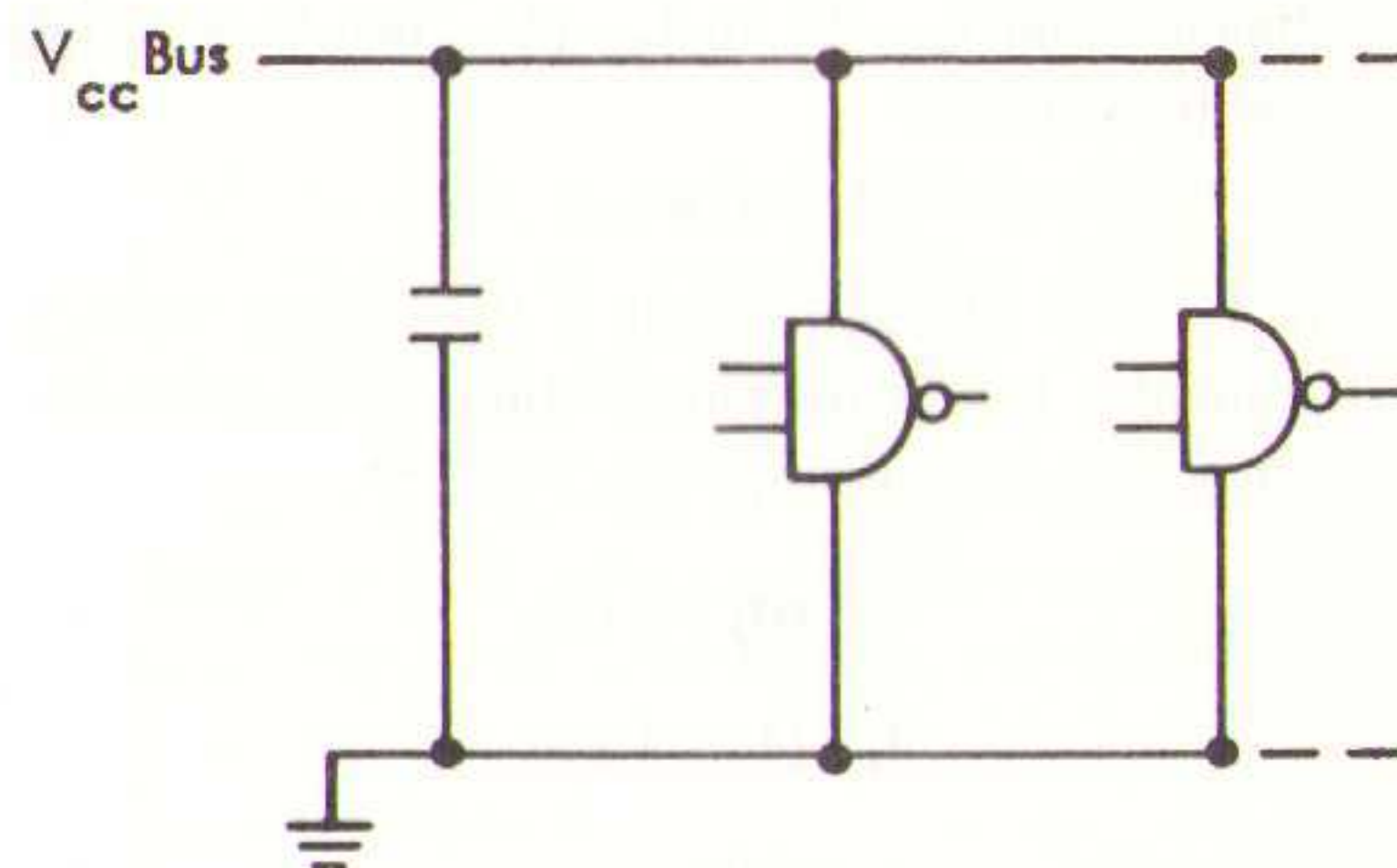


FIGURE 9. Capacitive Storage V_{CC} System

essentially d-c changes due to logic state changes coupled with transients associated with the change, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 10.

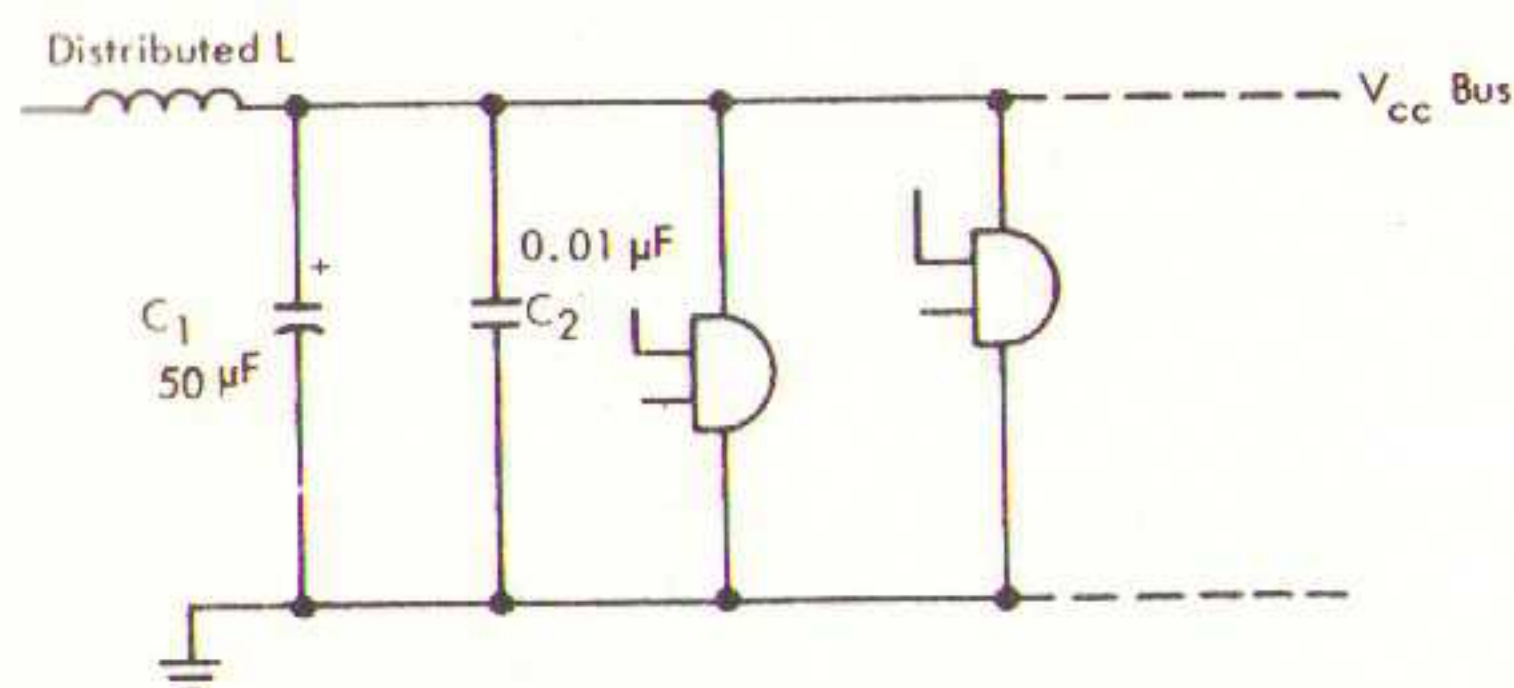


FIGURE 10. Commonly Used Power Distribution & Decoupling System

Typical component values may be found as follows:

For the RF capacitor, C2, assume the parameters to have common values such as

$$\Delta I_{cc} = 50 \text{ mA}$$

$$\Delta V \leq .1 \text{ V}$$

$$\Delta T = 20 \text{ ns}$$

$$C2 = \frac{\Delta I_{cc}}{\Delta V / \Delta T} = \frac{50 \times 10^{-3}}{.1 / (20 \times 10^{-9})} = \frac{(50)(20) \times 10^{-12}}{.1}$$

$$C2 = 10000 \times 10^{-12}$$

$$C2 = .01 \mu\text{F}$$

The same approach may be used for the low-frequency capacitor C1. However, the factor ΔT which was merely a worst case transient time when calculating C2 now becomes a bit hazy. An analysis of the current cycling on a statistical basis is the best approach in all but the simplest systems. The recommended procedure is to use "brute force," and decouple with 10 to 50 μF .

A discrete inductance of 2 to 10 microhenries is sometimes added for further decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients con-

fined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the V_{cc} line that do not force the gate output below the threshold level are not serious. Downward spikes as great as three volts have been tolerated on the V_{cc} line without propagating through the logic system. Thus the system designer can be greatly relieved on the subject of V_{cc} noise if even minimal consideration is given to the subject.

Ground noise is another matter. Pulses on the ground line can quite readily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. Likewise, if properly directed attention is paid to the ground system, problems seldom arise.

The concept of a common ground plane structure as used in RF and high-speed digital systems is quite different from that of the common ground point as used in low frequency circuits. The more closely the chassis and ground can approach being an integral unit, the better the noise suppression characteristics of the system. Consequently all parts of the chassis and ground bus system should be bound tightly together electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

The matter of grounds and decoupling on printed boards requires some attention here. The most desirable arrangement would be a double clad board with one side carrying the interconnections and the other a solid ground plane. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Crosstalk can become a problem on large boards; an adequate board ground mesh will go far in reducing crosstalk as well as ground noise. Some suggestions for board grounds where a plane is not practical are

1. Make the ground strap as wide as possible everywhere, even though this may mean its width varies radically.
2. Form a complete loop around the board, bringing both sides of the board through separate pins to the system ground.

The V_{cc} line can provide part of the ground mesh on the board, provided it is properly decoupled. For a

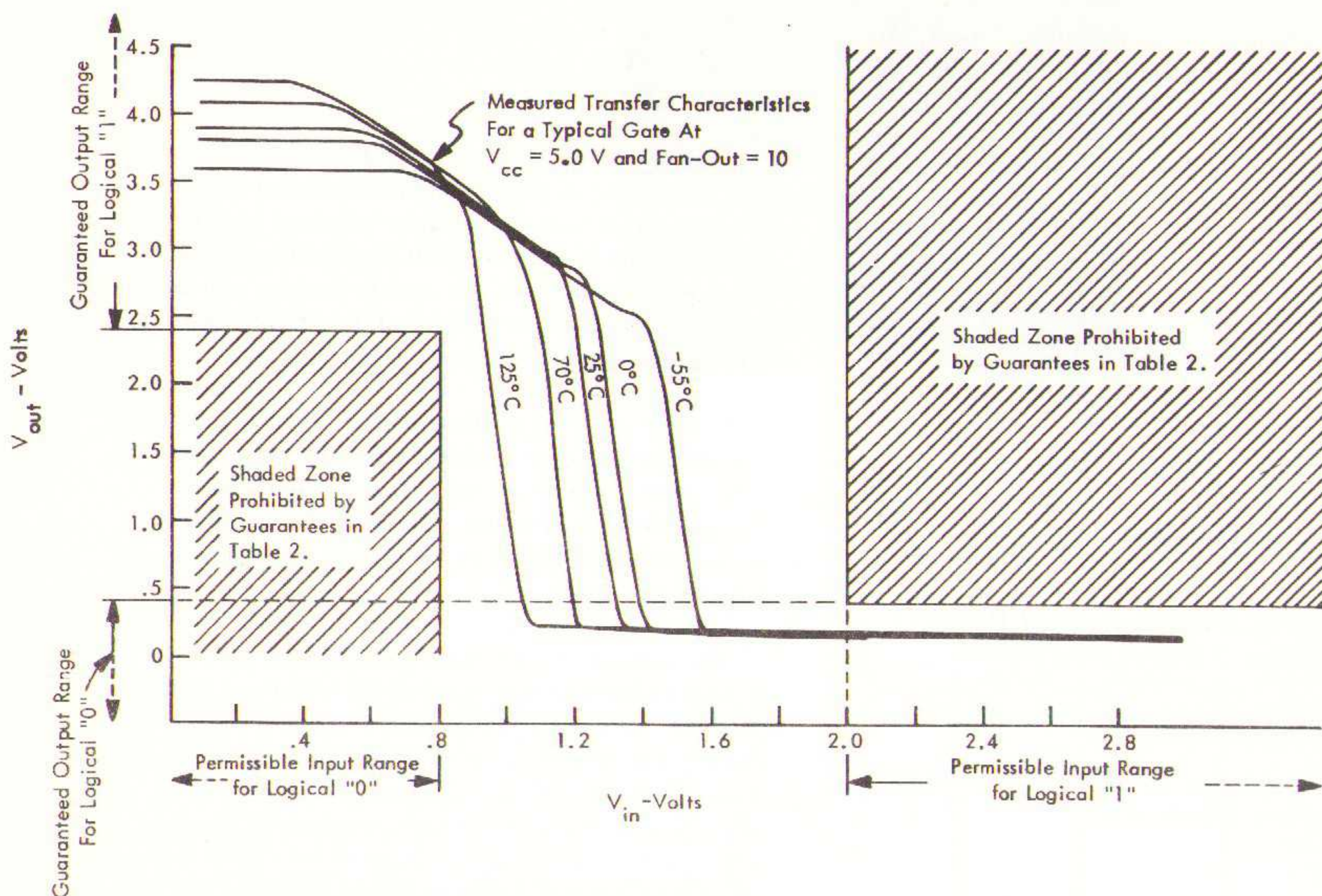


FIGURE 11. V_{out} vs. V_{in} Transfer Characteristics For SN5400/SN7400 Gates

TTL system, 0.01 μ F per synchronously driven gate, and at least .1 μ F per 20 gates regardless of synchronization is a good rule-of-thumb. This capacitance may be lumped, but is more effective if distributed over the board. A good rule to follow is to permit no more than five inches of wire between any package V_{cc} point; a total of 0.01 μ F, RF type capacitors are mandatory — disc ceramics are a good choice. It is sometimes a good practice to decouple the board from the external V_{cc} line with a 2.2 μ H inductor and a 10- μ F to 50- μ F capacitor as stated earlier, but this is optional, and the RF capacitors will still be required. In addition, it is strongly recommended that gates driving long lines have the V_{cc} supply decoupled at the gate V_{cc} terminal and that the capacitor, device ground, and transmission line ground be brought to a common point. The reasons for this should be more obvious after studying the currents involved in switching and line driving.

NOISE MARGIN IN 54/74 TTL

Intimately associated with noise performance are the inherent characteristics of the logic elements chosen for a given system. TTL circuits represent an excellent

composite of electrical properties for noise-free operation.

Figure 11 shows typical V_{out} vs. V_{in} characteristics for Texas Instruments SN5400/7400 gates.

By defining $V_{out(1)}$ as that output present when the input is a typical $V_{out(0)}$ level, $V_{out(0)}$ as that output present when the input is a typical $V_{out(1)}$ level, and $V_{threshold}$ as that voltage at which input and output are equal, it is possible to arrive at typical values for each. These are presented in Table 1. Note that these are not worst case definitions but operating values.

TABLE 1. Typical Output & Threshold Voltage for Texas Instruments SN5400/SN7400 Gates.

	$V_{cc} = 5.0$ V				
	-55°C	0°C	25°C	70°C	125°C
$V_{out(1)}$	3.6	3.8	3.9	4.1	4.25
$V_{out(0)}$	0.23	.24	0.25	.25	.25
V_{thresh}	1.49	1.33	1.26	1.15	1.1

In order to assure the user of Texas Instruments TTL a safe operating margin, the devices are tested and guaranteed to the data sheet limit⁽²⁾ shown in Table 2.

TABLE 2. *Guaranteed Input/Output Parameters for Texas Instruments SN5400/SN7400 Gates.*

$V_{out(1)}$	≥ 2.4 V
$V_{out(0)}$	≥ 0.40 V
$V_{in(1)}$	≥ 2.0 V
$V_{in(0)}$	≥ 0.80 V

The accepted definitions for d-c noise margins for the different logic states are defined in Figure 12. Now by examination of the data in Tables 1 and 2 the typical and worst case d-c noise margin curves for the SN5400/SN7400 series can be determined. Typical figures are illustrated graphically in Figure 13 for ambient temperatures from -55°C to $+125^{\circ}\text{C}$. The worst case guaranteed value of 400 millivolts⁽¹⁾ is a constant value within the above range covering both logic states for any load within the fanout limits of the device.

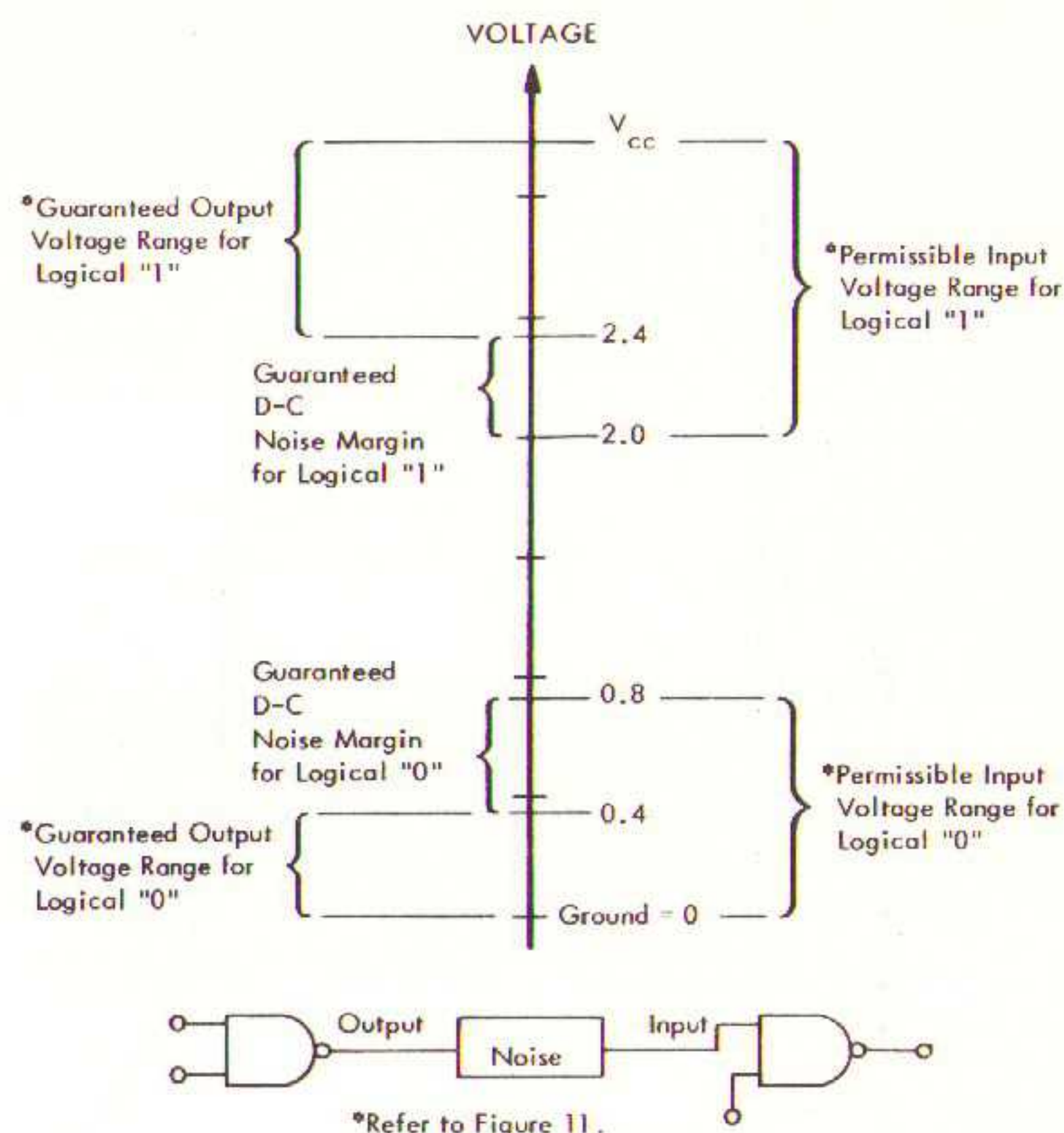


FIGURE 12. *Definition of Noise Margin for SN5400/SN7400 Gates*

In addition to the d-c noise immunity, a noise immunity may be defined around noise amplitude and pulse width. At the limits, the a-c noise immunity varies from the d-c values to a theoretical infinity at

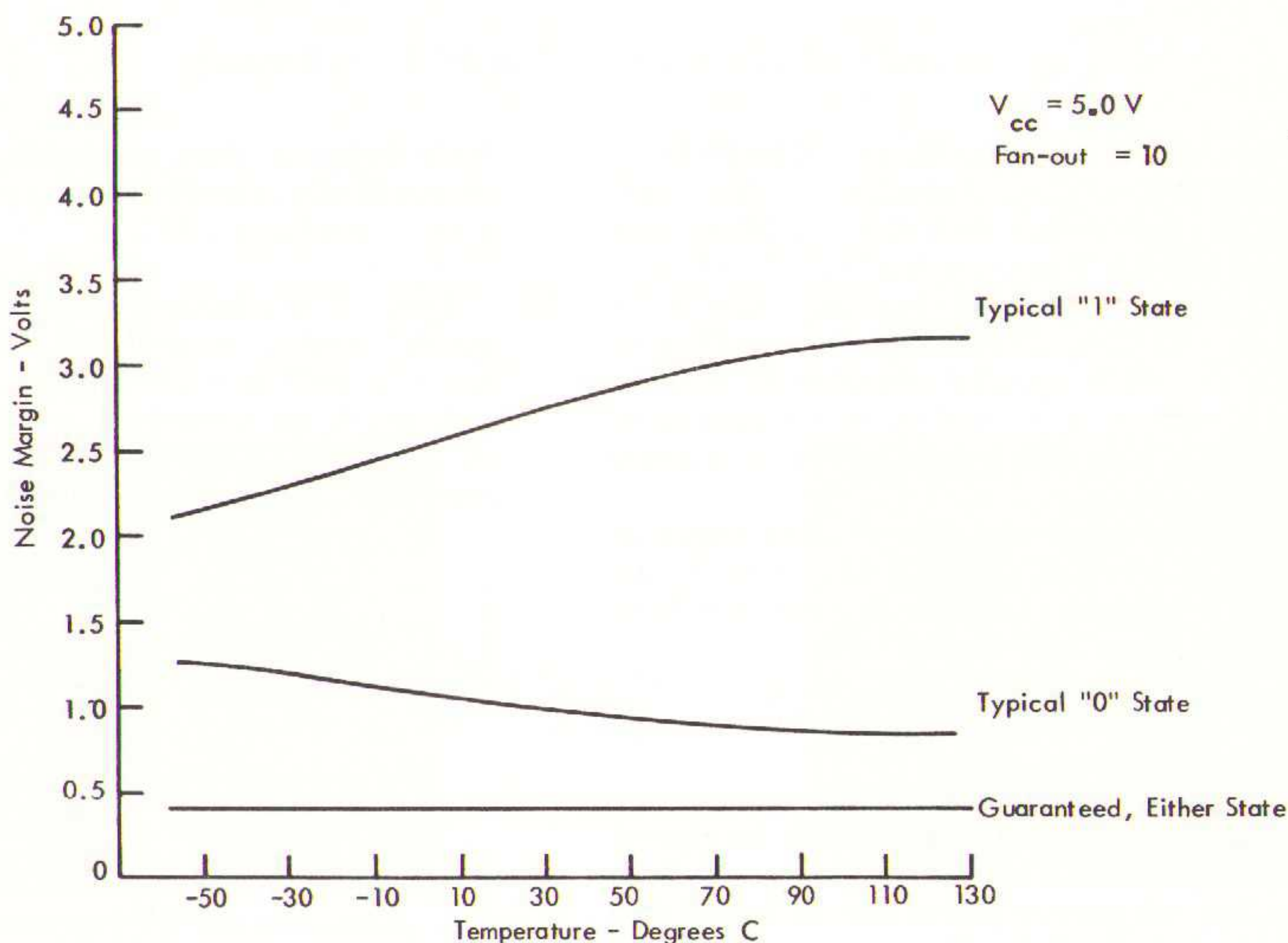


FIGURE 13. *SN5400/7400 DC Noise Margins*

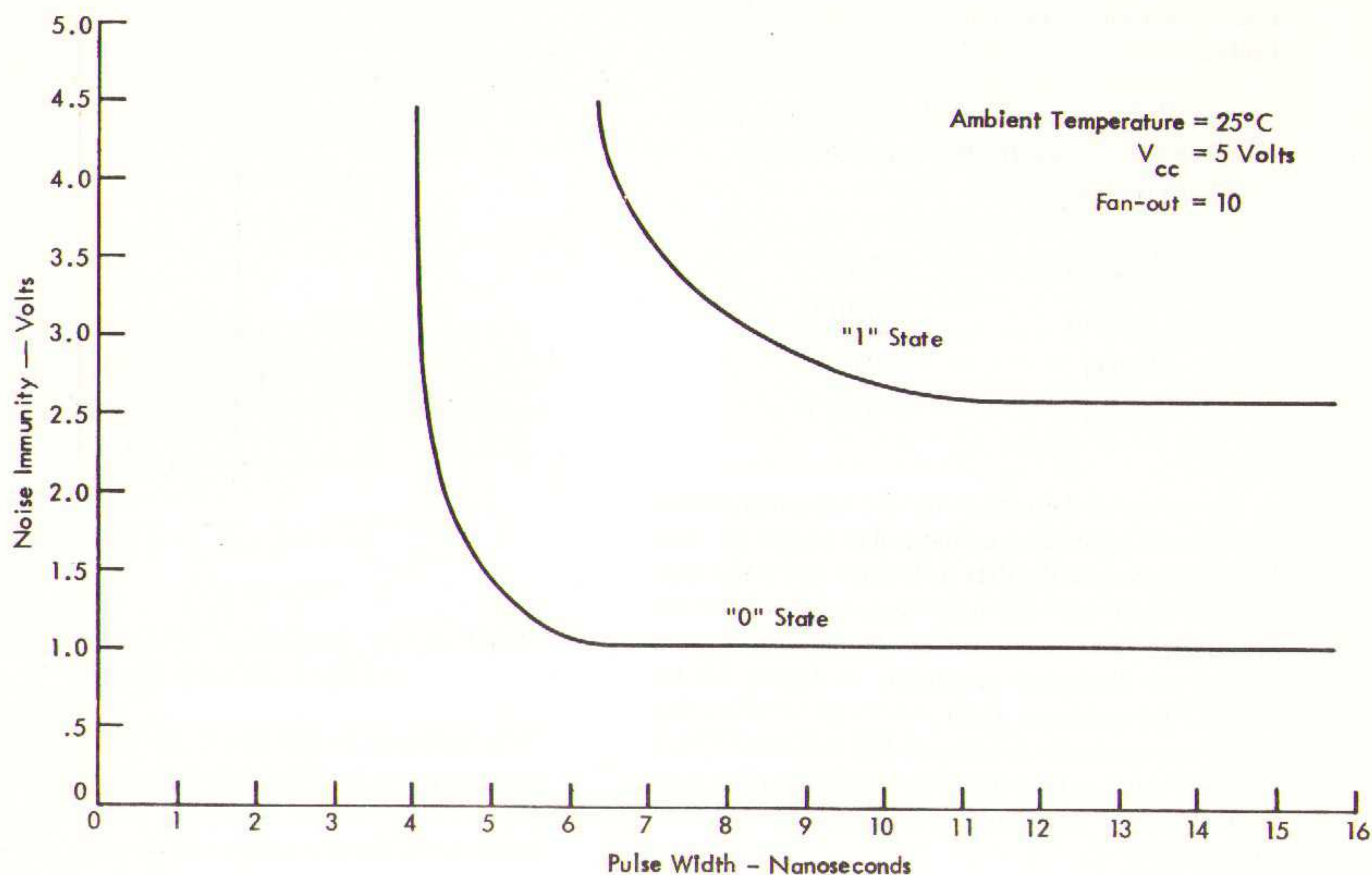


FIGURE 14. SN5400/SN7400 AC Noise Immunity

extremely narrow pulse widths as in Figure 14. Pulses shorter than the propagation delay of the devices will not propagate through the system. Thus the effective noise immunity is that noise level and pulse width below which noise signals will not propagate through the system. As shown in Figure 14, a-c noise rejection approaches infinity asymptotically at very narrow pulse widths and approaches the d-c noise margin asymptotically near pulse widths equal to device propagation delay.

In general, noise coupled from external sources has sufficient pulse width that only the d-c noise immunity is effective, since only about 6 nanoseconds are required for the device to respond.

CROSSTALK IN 54/74 TTL

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow creating linking magnetic fields. These cross-coupling effects are lumped together as "crosstalk."

Signal lines are grouped into three categories: coaxial lines, twisted pair lines, and straight wire lines.

Due to the low impedance and shielding characteristics of coaxial cable, coaxial cable cross talk is minimal and is no problem with TTL.

Figure 15 is adequately descriptive of practical types of signal transmission lines. The mutual reactances L_m and C_m which form the noise coupling paths, and the line parameters L_s and C_g which govern the Z_0 of the line will vary with the type line used. Since crosstalk is a function of the ratio of the mutual

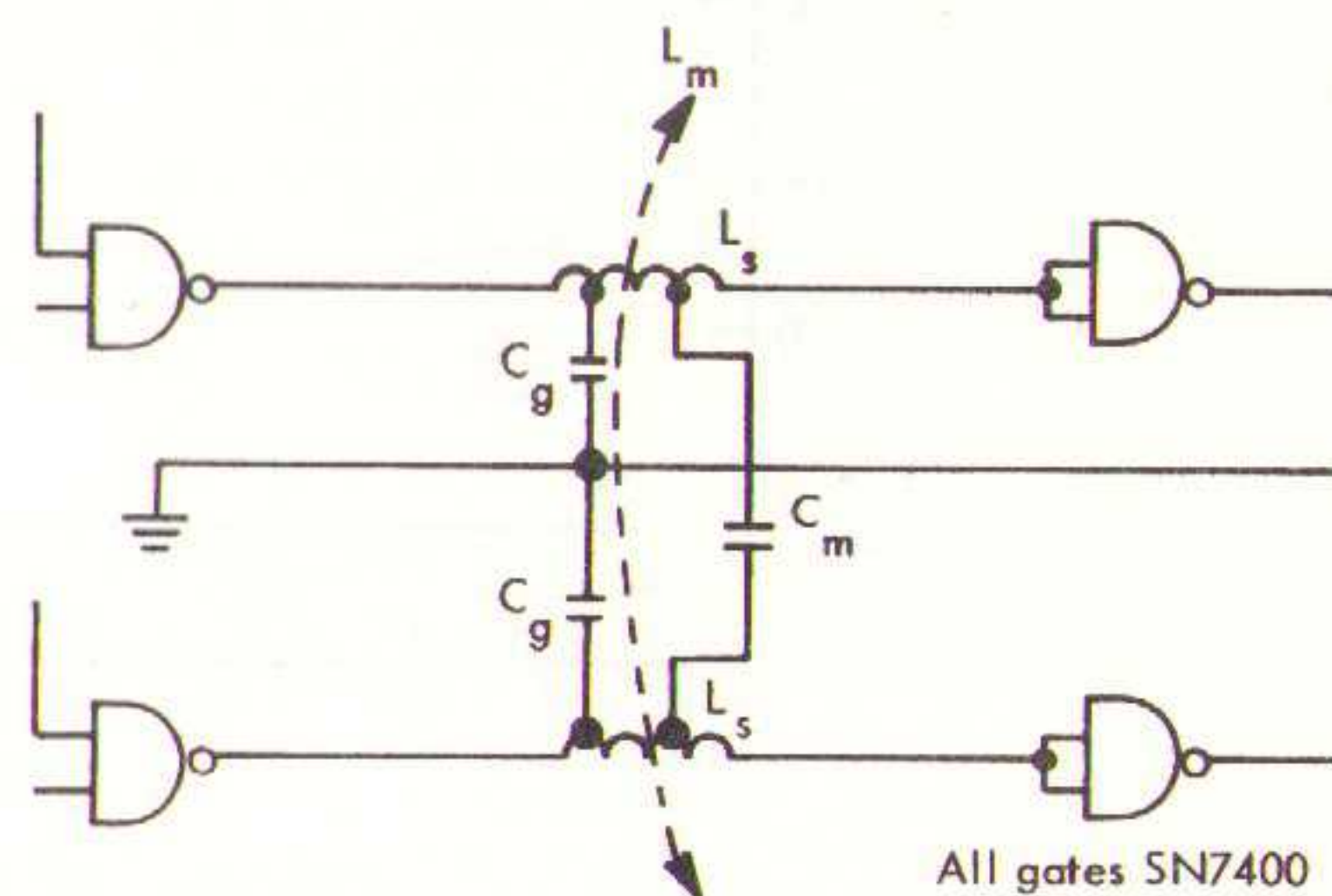


FIGURE 15. Coupling Impedances Involved In Crosstalk

impedances to the line characteristic impedances, the type of interconnection to be used must be at least partially a factor of crosstalk considerations. Coaxial cable combines very high mutual reactances with low characteristic impedances as well as shielding; therefore crosstalk is effectively eliminated. Twisted pair lines have higher characteristic impedances and lower coupling impedances; consequently crosstalk becomes a possible problem. Direct wired connections are the simplest and cheapest approach, but they are also the poorest for noise rejection.

Fortunately, much of the noise that may be coupled in is subdued by the very short time constants and impedance voltage-division which result from the low output impedances of SN5400/SN7400. It is possible to use direct leads up to ten inches, and up to twenty inches if the lead is routed close to ground and not cabled tightly together with similar leads. For longer distances twisted pair or coaxial cable is required. Twisted pairs are usually less expensive and easier to work with, but noise levels become objectionable beyond twelve feet.

An indication of the superior noise rejecting characteristics of SN5400/SN7400 TTL can be observed in the circuit in Figure 16. Although C_m is large (.001 μF) and C_g so small it can be neglected, capacitive crosstalk still does not appear. This leaves the designer with only inductive coupling effects to deal with.

LINE REFLECTIONS IN 54/74 TTL

When the lines used to transfer digital systems become long enough that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. Factors such

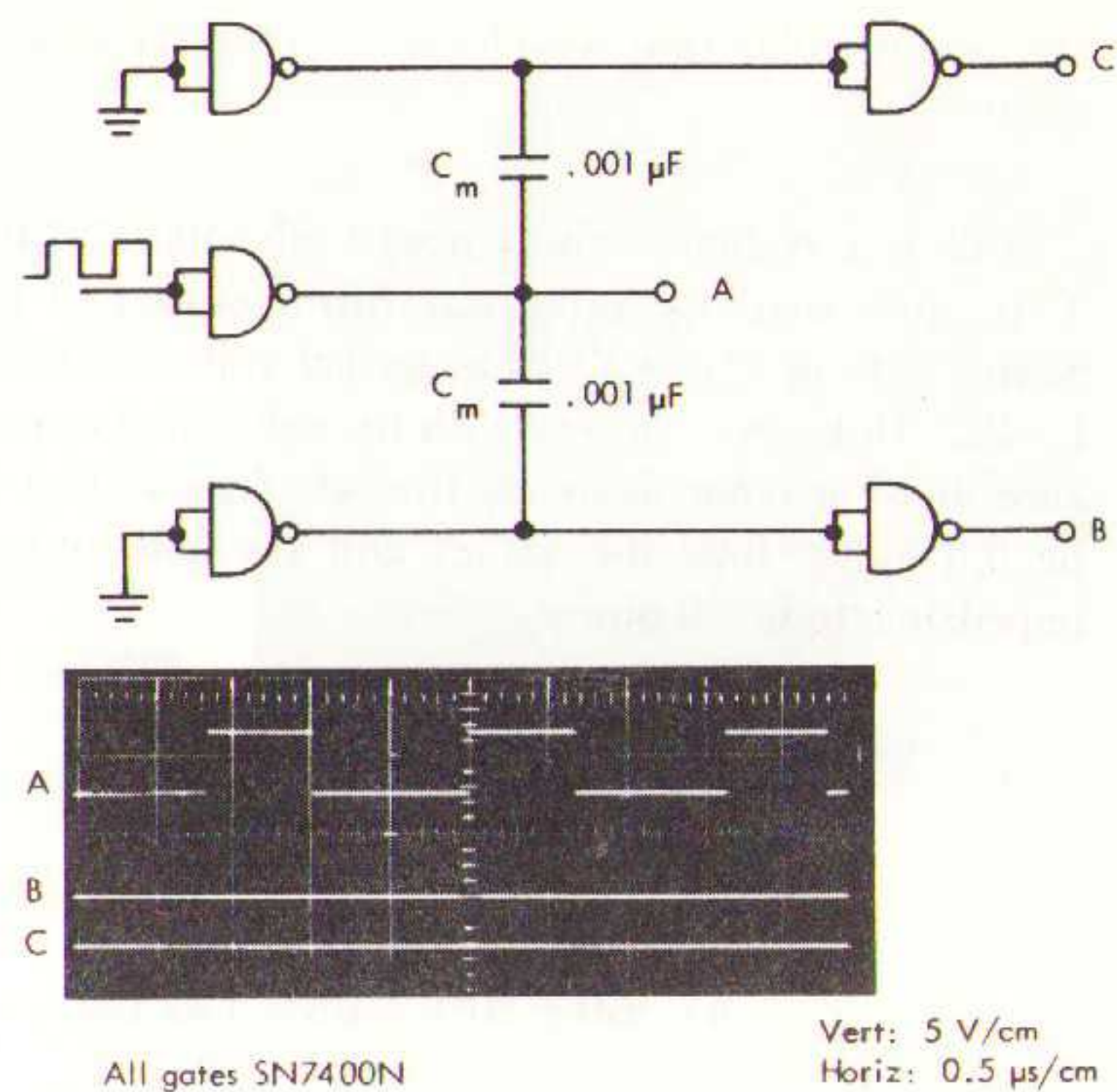
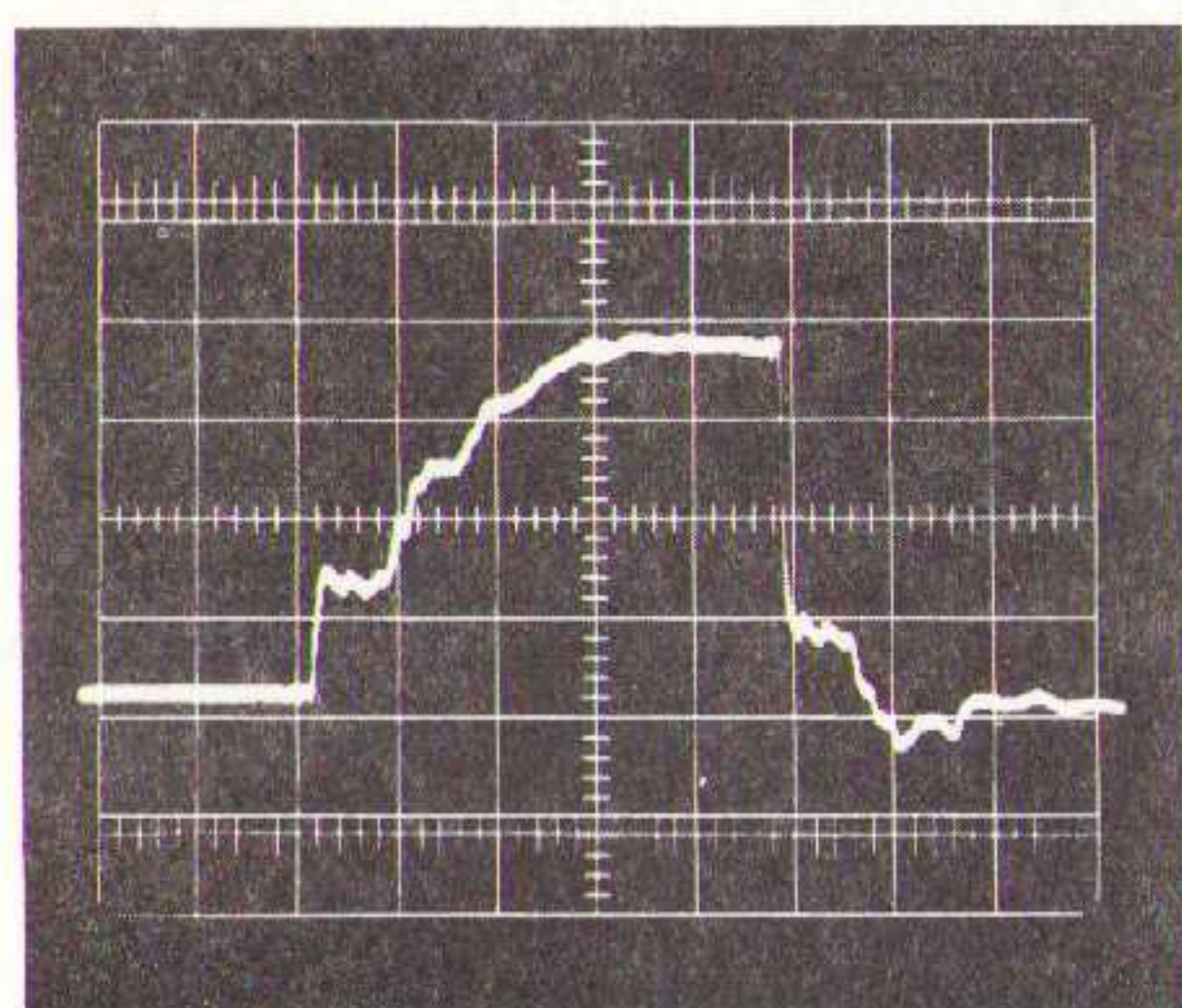


FIGURE 16. Static Crosstalk Immunity of SN5400/SN7400 TTL

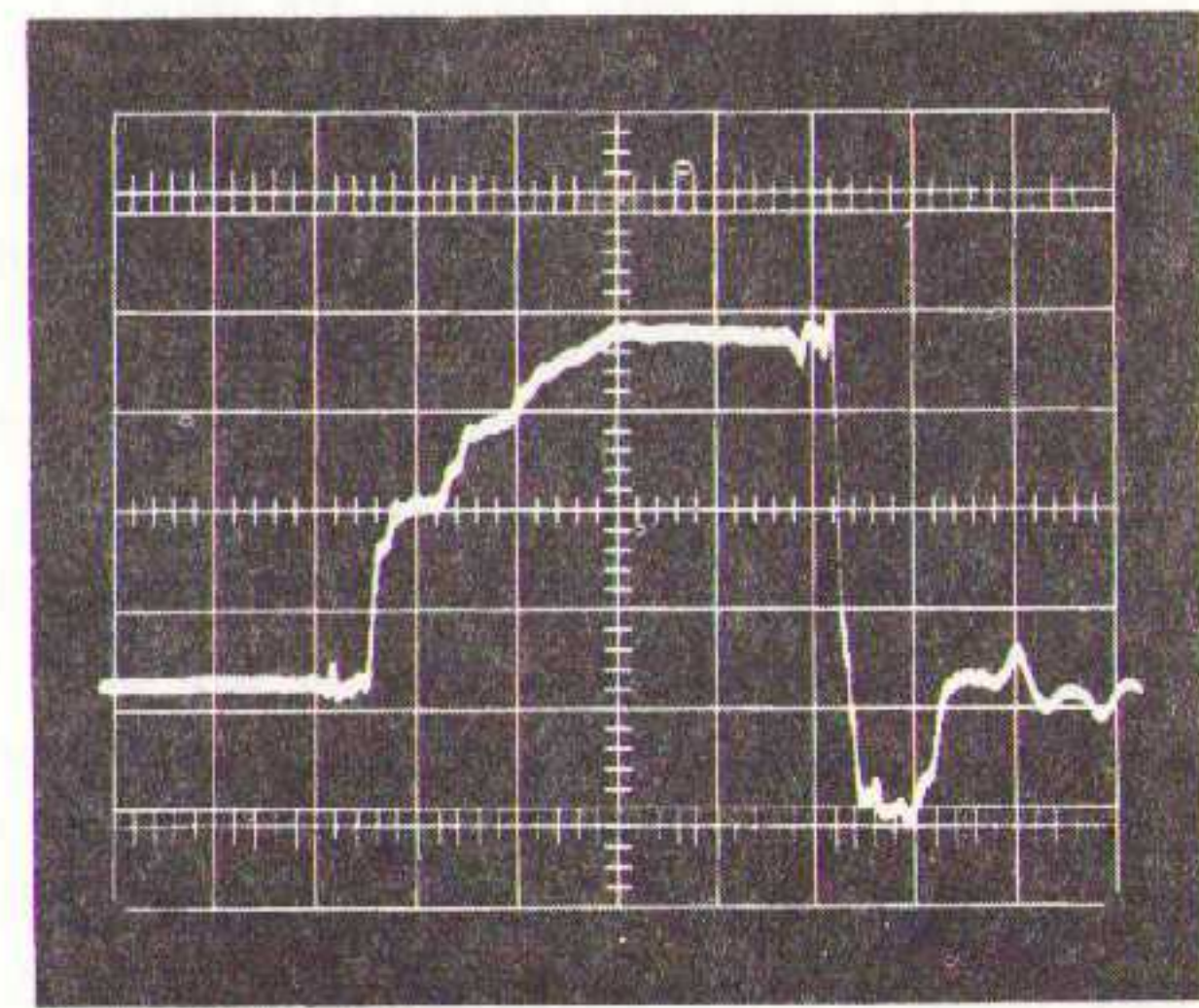
as gate output impedance, Z_o of the line, possible terminations, and line length must be evaluated since problems may arise in excessive delay, ringing, overshoot, or various other areas.

In the discussion related to Figure 3 note that only half the generator voltage was developed across the line initially, regardless of the termination. Assume the receiving end load, R , to be greater than Z_o , which is the only case normally encountered in SN5400/SN7400 TTL. The relative values of R and Z_o determine a positive reflection factor which sends the pulse back down the line to the receiving end after $2T$, where T is the time required for the signal to propagate the full length of the line. Figures 17a and b show



a. Line Input

Vert: 1 V/cm
Horiz: 100 ns/cm
 $Z_o = 50$
 $R_L = 1$ Unit Load



b. Line Output

FIGURE 17. Transmission Line Input & Output Waveforms With SN5400/7400, Figure 4

the input and output waveform for a test set up as in Figure 4.

This is a realistic situation with SN5400/SN7400 TTL. Note that the input waveform (output of the driving gate in Figure 5) steps to 1.4 volts and holds for 2T. This agrees closely with the calculated impedance division value, assuming the gate drive voltage to be 3.5 volts (final d-c value) and the gate output impedance to be 70 ohms:

$$\text{Voltage} = E \frac{Z_o}{Z_o + Z_s} + 3.5 \frac{50}{50 + 70} = 1.45 \text{ V}$$

The first step is terminated after 2T, at which time the first reflection from the load end returns and steps the voltage an additional 1.4 volts or a total of 2.8 volts. Additional steps occurring at 2T intervals bring the voltage up to the final d-c value, but since the second step is well above the minimum output "1" state, these steps are of little concern.

Looking to the load end (receiving gate input), the line input step is seen to arrive after T with an amplitude approximately double the input voltage calculated above. The actual received step level is seen to be 2.0 volts. Again these are approximately the anticipated values from transmission line theory.⁽¹⁾ The TTL gate input in the "1" state presents close to an open circuit termination.

The implications of these factors should be examined in detail. First, since the initial step at the line input falls at the threshold of a gate input (see Figure 11), any gate having its input connected to this point will be operating within its linear region and instability or oscillation could result. At the very best, its output state would be unknown. Also since the first step is so low, excessive currents are being drawn from the gate, aggravating ground and V_{CC} noise problems. At the receiving end, the first step does exceed the threshold and in fact reaches the guaranteed minimum output "1" level, but is seen to dip back to 2.2 volts with some loss of noise margin. If variations in devices, temperature, V_{CC} , and line impedance are considered, the situation looks much more critical. The receiving gate input could actually remain below the threshold on the first step. If so, an additional 2T delay is added, some undertermined amount of noise margin is lost, and instability could result as was pointed out for the driving end. Under other conditions the gate input

voltage could rise above the threshold and then fall below, causing a double pulsed output. Any number of possibilities could be uncovered by closer examination.

There is no one correction factor that will eliminate all those potential problems. A proper combination can be quite effective. Consider the following techniques.

To increase the amplitude of the input step:

1. Lower the driver impedance. Devices could be connected in parallel or the buffer gate used. In most cases neither is necessary with TTL.
2. Increase the transmission line impedance. Coaxial cables of 93 ohms are quite practical in size and cost; or twisted pairs can be used where practical. Twisted pair impedances vary from approximately 100 ohms upward.

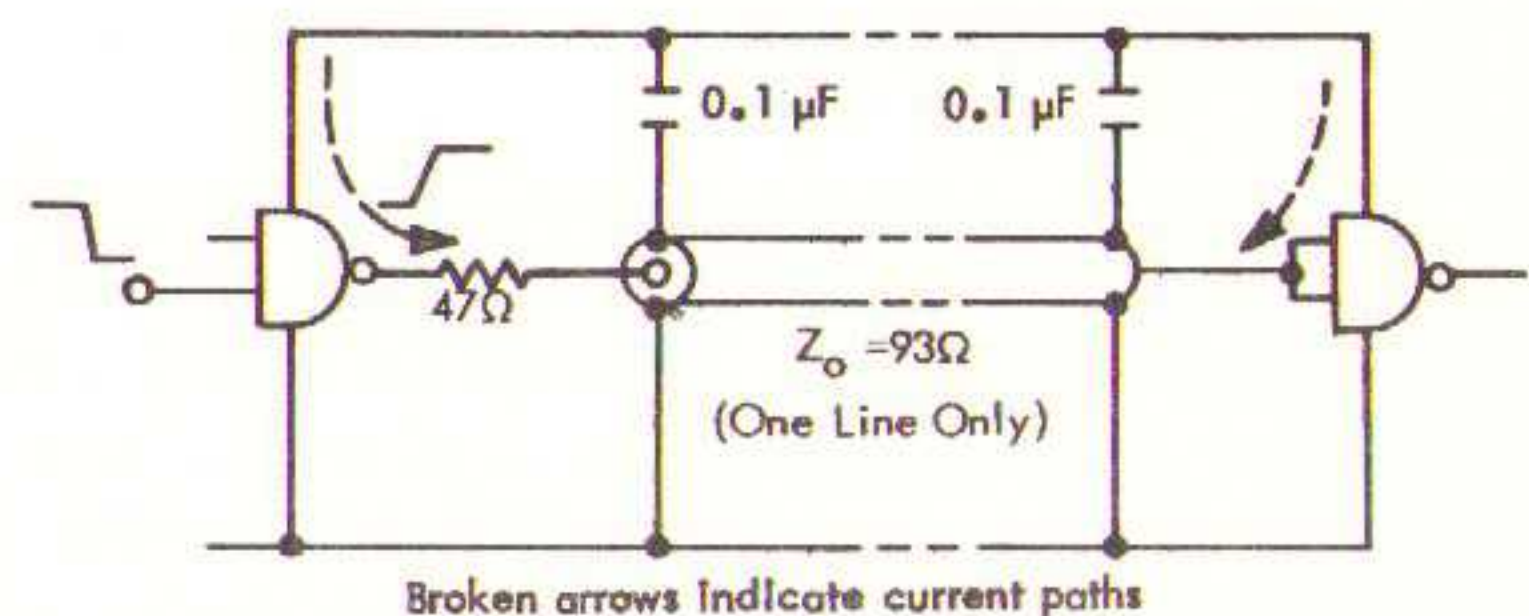
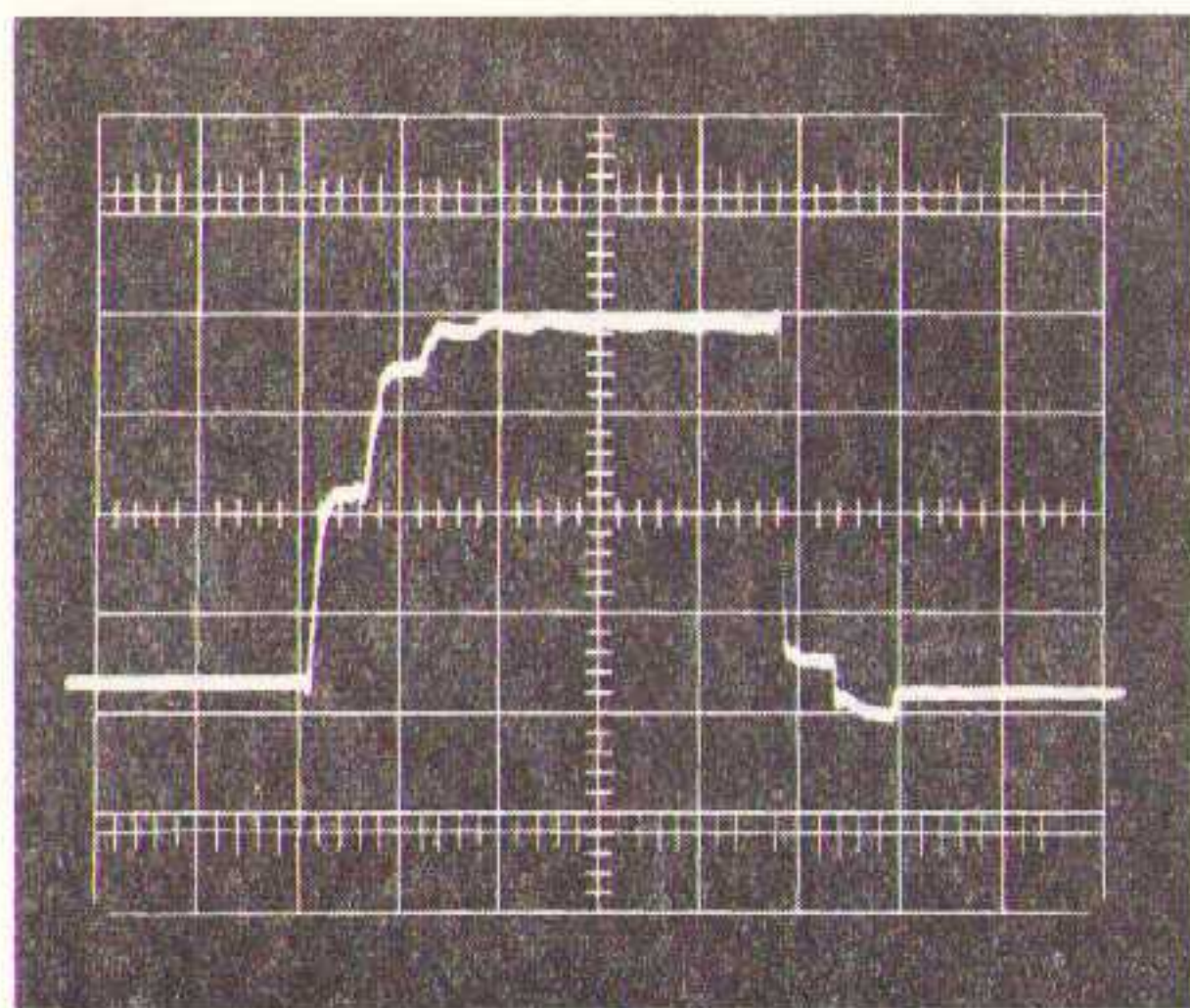


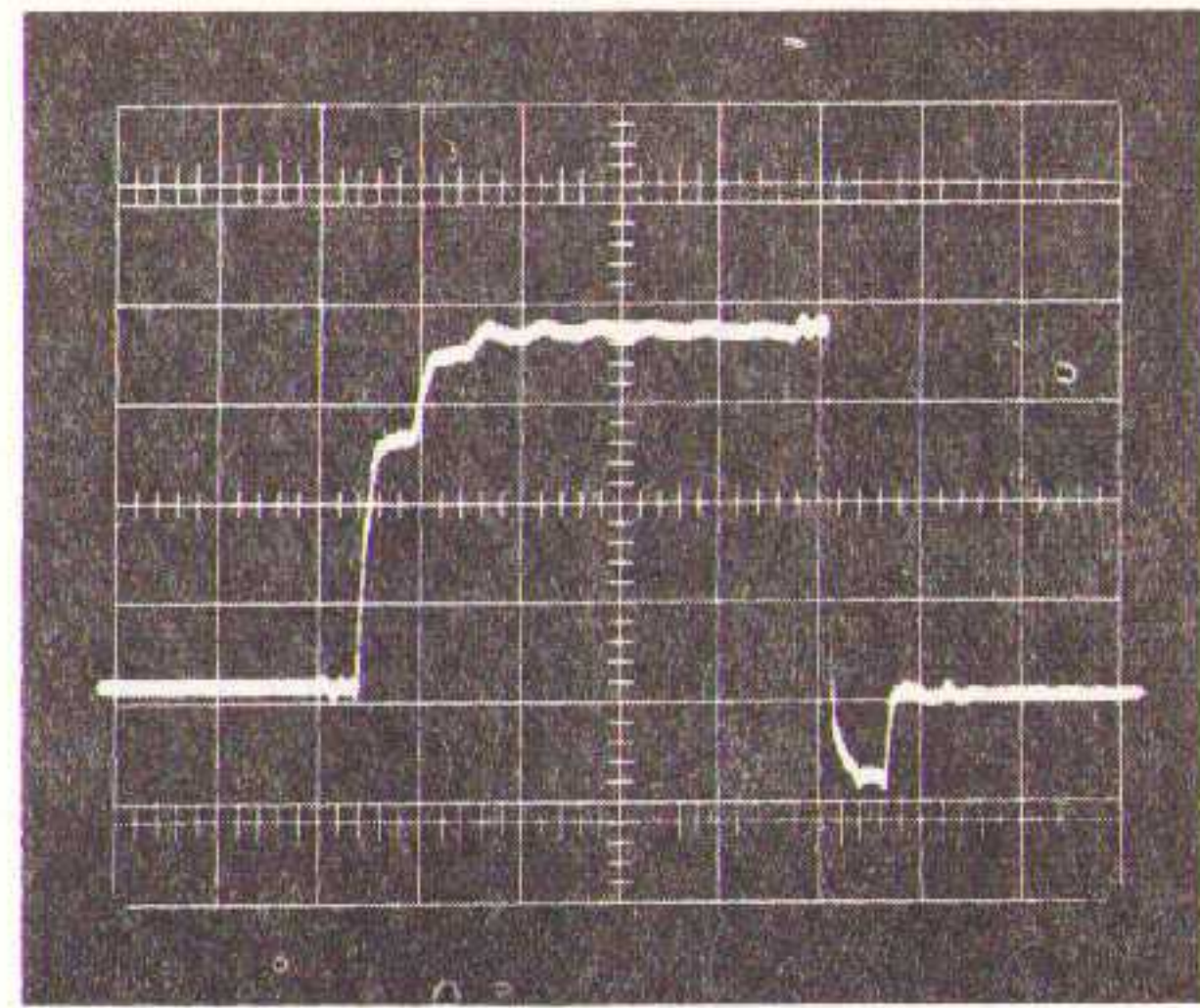
FIGURE 18. Recommended Line Driving And Receiving System

The second suggestion is implemented in Figure 18. Note the dramatic improvement of the waveform at both ends of the line shown in Figure 19. None of the potential problems noted before are likely now. However, it is still reasonable to put certain restrictions on the line driving capabilities and noise immunity of SN5400/SN7400 TTL:

1. Use direct wire interconnections that have no specific ground return for levels up to about ten inches only. A ground plane is always desirable.
2. Direct wire interconnections must be routed close to a ground plane if longer than ten inches, and should never be longer than twenty inches.
3. When using coaxial or twisted pair cables, design around approximately 100 ohms characteristic impedance. Coaxial cable of 93 ohms impedance (such as Microdot 293-3913) is recommended. For twisted pair, # 26 or # 28 wire with thin insulation twisted



a. Line Input



b. Line Output

Vert: 1 V/cm
Horiz: 100 ns/cm

FIGURE 19. Improved Waveforms Found in Circuit of Figure 18

about 30 turns per foot works well. Higher impedances increase crosstalk while lower impedances are difficult to drive.

4. Insure that transmission line ground returns are carried through at both transmitting and receiving ends.

5. Connect reverse termination at driver output to prevent negative overshoot.

6. Decouple line-driving and line-receiving gates as close to the package V_{CC} and ground pins as practical, with a .1- μ F capacitor.

7. Gates used as line drivers should be used for that purpose only. Gate inputs connected directly to a line driving output could receive erroneous inputs due to line reflections, long delay times introduced, or excessive loading on the driving gate.

8. Gates used as line receivers should have all inputs tied together to the line. Other logic inputs to the receiving gate should be avoided and a single gate should be used as the termination of a line.

9. Flip-Flops are generally unsatisfactory line drivers due to the possibility of collector commutation from reflected signals.

SUMMARY

Since SN5400/SN7400 devices characteristically have short propagation delay times with fast rise and fall times it might be assumed that TTL devices have poor system noise characteristics. However, between the noise producing output and the noise receiving input lies the efficiency of the noise coupling. It is in

this area that the most outstanding characteristic of TTL is applied. The SN5400/SN7400 inputs are voltage level (and pulse width) sensitive. Obviously then, the extremely low output impedances in the "0" and "1" states minimize the coupling time constant and are a tremendous factor in reduction of cross coupling. In practice this offsets the shorter delay times and faster rise and fall times of TTL which tend to increase cross coupling. Thus TTL will often be found to perform well in systems where devices with slower transistions or higher DC margins but with higher impedances are ineffective.

The undesired effects of noise in a digital system can be essentially eliminated by proper system design considerations. Texas Instruments SN5400/SN7400 TTL has been shown to possess the high noise margins and low impedances desirable in combating noise. In industrial systems, the additional speed of TTL shows no greater susceptibility to environmental noise than slower devices.

Crosstalk and line reflections are easily handled with TTL if the high frequency characteristics and low impedances are considered. Cabling and grounding/decoupling must be done as for an RF system. Proper attention to the measures discussed in this report produces a system of superior performance compared to those using less sophisticated logic devices.

REFERENCES

- (1) Stewart, John L., *Circuit Analysis of Transmission Lines*, John Wiley & Sons, pp. 23-42.
- (2) Texas Instruments Incorporated, "1967-68 Integrated Circuits Catalog," pp. 1002.

TTL LOADING DATA

normalized fan-out

Fan-out capabilities shown on the individual data sheets in this catalog have been normalized to reflect the circuits ability to supply a load or sink current to a number (N) of selected unit loads. In each of the three TTL families, the selected unit load consists of a circuit representative of the worst-case current required to drive one emitter of the multiple-emitter, input transistor characteristic of that family. A summary of the values used for normalizing is shown in Table I. Figures 1 and 2 illustrate the direction of the currents.

Table I. Values Used for Normalizing

SERIES	OUTPUT STATE	CHARACTERISTICS		FAN-OUT (SEE NOTE 1)	
		STANDARD TOTEM-POLE OR DARLINGTON OUTPUT	EACH STANDARD INPUT EMITTER	ACTUAL	NORMALIZED
54/74	Logical 1	$I_{load} = -400 \mu A$, $V_{out(1)} = 2.4 V$ min	$I_{in(1)} = 40 \mu A$ max @ $V_{in} = 2.4 V$	10	10
	Logical 0	$I_{sink} = 16 mA$, $V_{out(0)} = 0.4 V$ max	$I_{in(0)} = 1.6 mA$ max @ $V_{in} = 0.4 V$	10	10
54H/74H	Logical 1	$I_{load} = -500 \mu A$, $V_{out(1)} = 2.4 V$ min	$I_{in(1)} = 50 \mu A$ max @ $V_{in} = 2.4 V$	10	10
	Logical 0	$I_{sink} = 20 mA$, $V_{out(0)} = 0.4 V$ max	$I_{in(0)} = -2 mA$ max @ $V_{in} = 0.4 V$	10	10
54L/74L	Logical 1	$I_{load} = -100 \mu A$, $V_{out(1)} = 2.4 V$ min	$I_{in(1)} = 10 \mu A$ max @ $V_{in} = 2.4 V$	10	10*
	Logical 0	$I_{sink} = 2 mA$, $V_{out(0)} = 0.3 V$ max	$I_{in(0)} = -18 mA$ max @ $V_{in} = 0.3 V$	>11	10*

NOTE 1: Actual fan-out values shown here are: Logical 1 fan-out = $I_{load} \div I_{in(1)}$
Logical 0 fan-out = $I_{sink} \div I_{in(0)}$
* Limiting parameter is I_{load} of driving circuit.

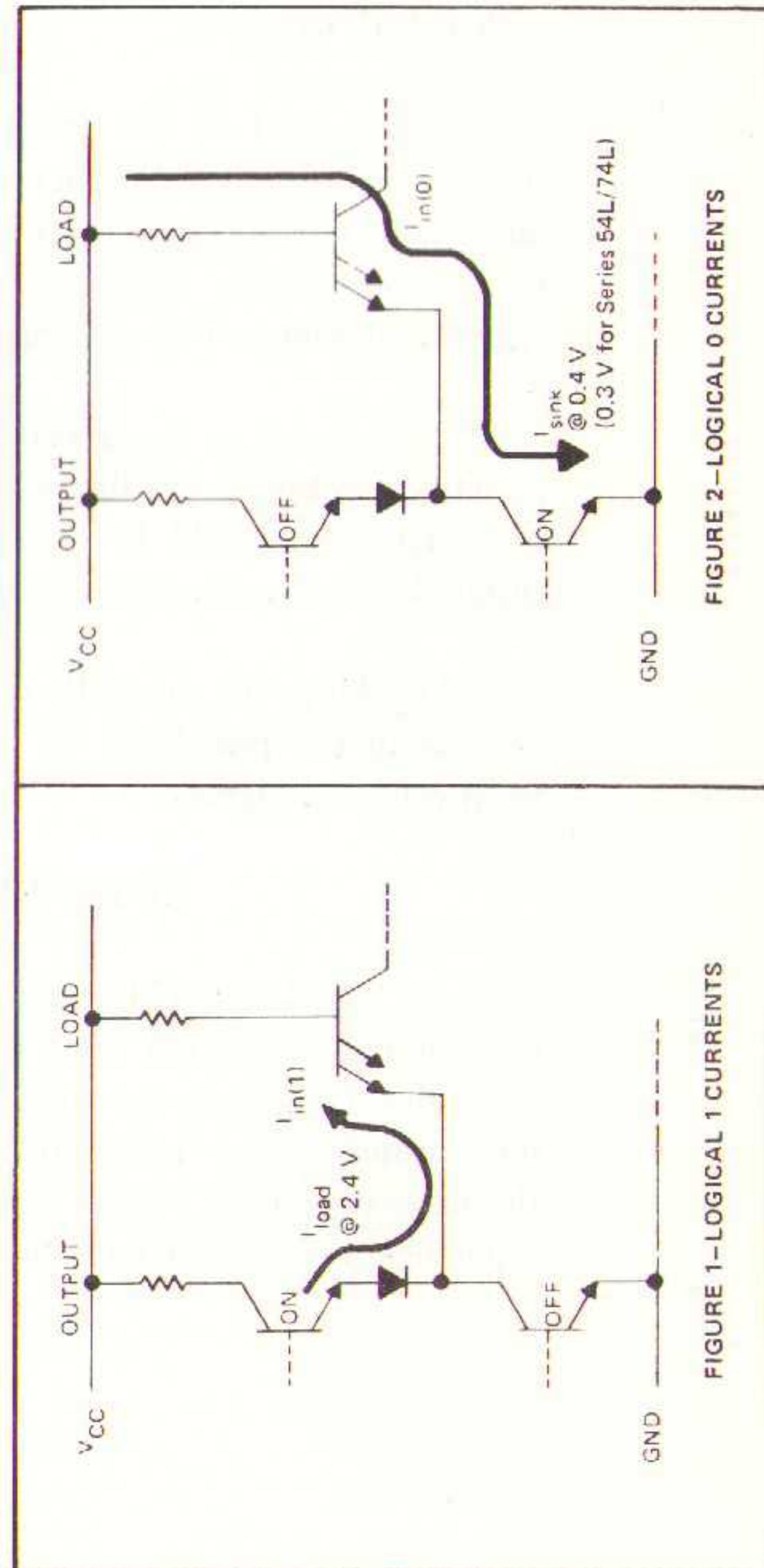


FIGURE 1—LOGICAL 1 CURRENTS

FIGURE 2—LOGICAL 0 CURRENTS

termination of unused inputs

Input current requirements for multiple emitters of the same input transistor which are connected so as to be driven by the same output are detailed in Table II.

Table II. Input Currents When Emitters are Tied Together

NUMBER OF EMITTERS TIED TOGETHER	TOTAL INPUT CURRENT REQUIRED	
	$I_{in(0)}$	$I_{in(1)}$
1	$1 \times I_{in(0)}$	$1 \times I_{in(1)}$
2	$1 \times I_{in(0)}$	$2 \times I_{in(1)}$
3	$1 \times I_{in(0)}$	$3 \times I_{in(1)}$
...	...	...
N	$1 \times I_{in(0)}$	$N \times I_{in(1)}$

This merely illustrates the fact that when unused inputs are tied to used inputs, only the $I_{in(1)}$ current requirements are increased. Most new TTL MSI circuits are characterized to drive 20 normalized logical 1 level loads to simplify the termination of unused inputs to used inputs.

combining standard, high-speed, and low-power circuits

Since various sections of digital logic systems have different speed requirements, a considerable improvement in system efficiency is realized when all three speed/power ranges of TI's compatible TTL are utilized. For example, Series 54H/74H high-speed circuits may be employed in critical arithmetic sections, while standard-speed Series 54/74 and Series 54L/74L SSI and MSI circuits can be selectively used without degradation in system performance (and without special interface circuits) to minimize power consumption.

The most efficient calculations for maximum fan-out when mixing standard, high-speed, and low-power TTL circuits are achieved by using the actual current values. As an example, consider a Series 54L/74L gate (see Figure 3) driving one Series 54/74 load (A), two Series 54L/74L loads (B and C), and four unused emitters (B₁, B₂, C₁, and C₂, two on each of the 54L/74L input transistors, B and C). The calculations are shown in Table III.

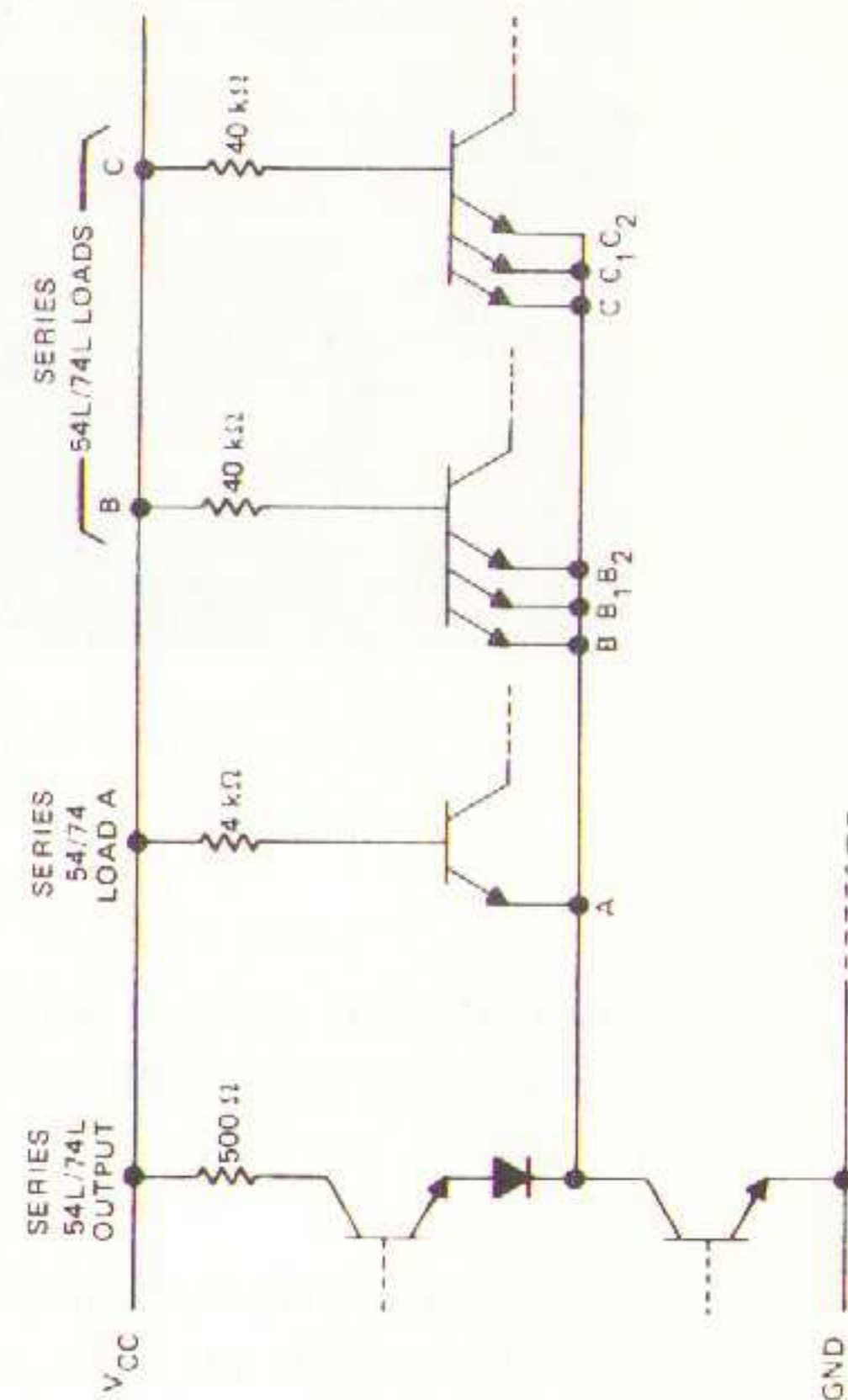


FIGURE 3

Table III. Examples of Calculating Maximum Fan-Out (Series 54L/74L)

AVAILABLE DRIVE	LOADS
$I_{load} = 100 \mu A$	$I_{in(1)} = 40 \mu A$
$I_{sink} = 2 mA$	$I_{in(0)} = 1.6 mA$
	$I_{in(1)} = 10 \mu A$
	$I_{in(0)} = 0.18 mA$
	$I_{in(1)} = 10 \mu A$
	$I_{in(0)} = 0.18 mA$
	$I_{in(1)} = 10 \mu A$
	$I_{in(0)} = 0.18 mA$
	$I_{in(1)} = 10 \mu A$
	$I_{in(0)} = 0.18 mA$
	$I_{in(1)} = 10 \mu A$
	$I_{in(0)} = 0.18 mA$
Less Total	$100 \mu A$
Load Values: $100 \mu A$	$1.96 mA$
0	$0.04 mA$

This illustrates the fact that a Series 54L/74L output will actually drive any combination of logical 1 and logical 0 loads which does not exceed its rating of 100- μA logical 1 drive and 2-mA logical 0 drive. The combination could just as well have been one Series 54/74 logical 0 level load, two Series 54/74 logical 1 level loads, and two Series 54L/74L loads.

Table IV. Actual D-C Fan-Out Capabilities

SERIES 54/74	DRIVING	SERIES 54H/74H	
$I_{load} = 400 \mu A \div 50 \mu A = 8$ loads		$I_{in(0)} = 1.6 mA$	54H/74H and 54L/74L Normalized to 54/74
$I_{sink} = 16 mA \div 2 mA = 8$ loads			
SERIES 54/74	DRIVING	SERIES 54L/74L	
$I_{load} = 400 \mu A \div 10 \mu A = 40^*$ loads		$I_{in(0)} = 0.18 mA$	54/74 and 54L/74L Normalized to 54H/74H
$I_{sink} = 16 mA \div 0.18 mA = 88.8$ loads			
SERIES 54H/74H	DRIVING	SERIES 54/74	
$I_{load} = 500 \mu A \div 40 \mu A = 12.5$ loads		$I_{in(0)} = 1.6 mA$	54/74 and 54L/74L Normalized to 54L/74L
$I_{sink} = 20 mA \div 1.6 mA = 12.5$ loads			
SERIES 54H/74H	DRIVING	SERIES 54L/74L	
$I_{load} = 500 \mu A \div 10 \mu A = 50^*$ loads		$I_{in(0)} = 0.18 mA$	54/74 and 54L/74H Normalized to 54L/74L
$I_{sink} = 20 mA \div 0.18 mA = 111.1$ loads			
SERIES 54L/74L	DRIVING	SERIES 54/74	
$I_{load} = 100 \mu A \div 40 \mu A = 2.5$ loads		$I_{in(0)} = 1.6 mA$	54/74 and 54L/74H Normalized to 54L/74L
$I_{sink} = 2 mA \div 1.6 mA = 1.25^{\dagger}$ loads			
SERIES 54L/74L	DRIVING	SERIES 54H/74H	
$I_{load} = 100 \mu A \div 50 \mu A = 2$ loads		$I_{in(0)} = 1.6 mA$	54/74 and 54L/74H Normalized to 54L/74L
$I_{sink} = 2 mA \div 2 mA = 1^{\dagger}$ load			

* Limiting parameter is I_{load} of driving circuit.
 $\dagger$ Limiting parameter is I_{sink} of driving circuit.

generalized loading rules for the TTL families

Attempts to normalize the three families to a single set of fan-out numbers result in the apparent loss of some drive capability when compared to the calculations using actual current values. In addition, to be usable, the group of generalized fan-out numbers should be a small group of easily remembered values. A look at the actual normalized fan-out capability of each TTL family, when compared to input current requirements of the other two families, is provided in Table IV.

It is obvious that this group of values would be difficult to remember; however, these numbers do serve as a reference for logical 1 and logical 0 fan-out based on actual current values when the loads to be driven are all of the same family.

To develop a set of generalized loading rules which will determine fan-out from either of the three types of outputs to mixed loads consisting of any combination of 54/74, 54H/74H, or 54L/74L loads, it is necessary to ratio the various input current requirements and fan-out capabilities to the same constant. Ideally, the results will be a single set of numbers which are applicable for both logical 1 and logical 0 fan-out conditions. Testing various formulas proved that generalizing input current requirements and drive capabilities to Series 54/74 values best filled these requirements. The calculations are explained in Table V.

Table V. Ratio Calculations

LOGIC FAMILY	INPUT CURRENT REQUIREMENTS		FAN-OUT CAPABILITIES	
	Logical 1 (Base = μA)	Logical 0 (Base = μA)	Logical 1 (Base = μA)	Logical 0 (Base = μA)
Series 54/74	$40 \div 40 = 1$	$1.6 \div 1.6 = 1$	$400 \div 40 = 10$	$16 \div 1.6 = 10$
Series 54H/74H	$50 \div 40 = 1.25$	$2 \div 1.6 = 1.25$	$500 \div 40 = 12.5$	$20 \div 1.6 = 12.5$
Series 54L/74L	$10 \div 40 = 0.25$	$0.18 \div 1.6 = 0.112$	$100 \div 40 = 2.5^{\dagger}$	$2 \div 1.6 = 1.25^{\ddagger}$

$\ddagger$ Limiting parameter varies depending on type of loads driven.

When the limiting parameter of each family is considered with respect to the other two families, these ratios produce the generalized numbers listed in Table VI.

Table VI. Generalized Loading Factors

INPUT LOAD FACTOR	SERIES	OUTPUT LOAD FACTOR		
		TO SERIES 54/74	TO SERIES 54H/74H	TO SERIES 54L/74L
1	54/74	10	10	10*
1.25	54H/74H	12.5	12.5	12.5*
0.25	54L/74L	1.25 $\dagger$	1.25 $\dagger$	2.5*

* Limiting parameter is I_{load} of driving circuit.
 $\dagger$ Limiting parameter is I_{sink} of driving circuit.

When each generalized input load factor (first column) is used to determine fan-out to loads of the same family (shaded boxes), the result in each case is 10, the same normalized value used on the data sheets.

Examples:

	Input Load Factor	Output Load Factor	Fan-Out
Series 54/74	1	10	10
Series 54H/74H	1.25	12.5	10
Series 54L/74L	0.25	2.5	10

Further examination indicates that when these generalized load factors are used to determine fan-out to mixed loads (output load factor $\div$ input load factor, see Table VII), the maximum loads obtained are the same as the actual d-c fan-out of the limiting parameter shown in Table IV.

TTL LOADING DATA

The most significant variation between actual and generalized fan-out capabilities occurs when Series 54L/74L outputs are used to drive Series 54/74 and 54L/74L inputs. The generalized numbers indicate that the Series 54L/74L output will drive only one Series 54/74 load and one Series 54L/74L load simultaneously. Calculations in Table III indicate that a Series 54L/74L output will drive at least one Series 54/74 load and two Series 54L/74L loads.

Series 54/74 Input Load Factor	1
Series 54L/74L Input Load Factor	(+) 0.25
Series 54L/74L Output Load Factor	1.25

When Series 54L/74L is used to drive 54L/74L loads, the generalized fan-out number for 54L/74L outputs is actually twice as large as when driving Series 54/74 or 54H/74H loads. This can easily be compensated for by:

- a. Doubling the Series 54/74 or 54H/74H input load factor and using 2.5 as fan-out capability for Series 54L/74L.

Example:

Input Load Factor— Series 54/74 2 (one load doubled)	
Input Load Factor— Series 54L/74L (+) 0.50 (two 0.25 loads)	
Output Load Factor— Series 54L/74L 2.50	

- b. Or, double the remaining Series 54L/74L output load factor after subtracting Series 54/74 loads.

Example:

Output Load Factor— Series 54L/74L 1.25	
Input Load Factor— Series 54/74 (-) 1	
Remaining Output Load Factor— Series 54L/74L 0.25	
Double 0.25 X 2 = 0.50	
Input Load Factor— Series 54L/74L 0.50 (two 0.25 loads)	0

Table VII. Generalized D-C Fan-Out Capabilities To Mixed Loads

SERIES 54/74	DRIVING SERIES 54H/74H	$10 \div 1.25 = 8$ (A)	54H/74H and 54L/74L Normalized to 54/74
SERIES 54H/74H	DRIVING SERIES 54L/74L	$10 \div 0.25 = 40$ (B)	
SERIES 54H/74H	DRIVING SERIES 54L/74L	$12.5 \div 1 = 12.5$ (C)	54/74 and 54L/74L Normalized to 54H/74H
SERIES 54H/74H	DRIVING SERIES 54L/74L	$1.25 \div 0.25 = 50$ (D)	
SERIES 54L/74L	DRIVING SERIES 54/74	$1.25 \div 1 = 1.25$ (E)	54/74 and 54H/74H Normalized to 54L/74L
SERIES 54/74	DRIVING SERIES 54/74	$1.25 \div 1.25 = 1$ (F)	

These fan-out rules are very useful for tabulating loading of outputs. However, if these maximums are reached for a particular output, it will be advantageous if the actual current values are considered, especially if loads remain which could be driven within the allowable maximum. A detailed listing of generalized load and fan-out factors for inputs and outputs of the 74, TTL families is provided in Tables VIII.

Table VIII. Series 54/74 Generalized Loading Factors

SERIES 54/74				
Device	Location	Input Load Factor	Output Load Factor	
SN5400/7400	Any Input Any Output	1.0	10.0	
SN5401/7401	Any Input Any Output	1.0	10.0	
SN5402/7402	Any Input Any Output	1.0	10.0	
SN5403/7403	Any Input Any Output	1.0	10.0	
SN5404/7404	Any Input Any Output	1.0	10.0	
SN5405/7405	Any Input Any Output	1.0	10.0	
SN5410/7410	Any Input Any Output	1.0	10.0	
SN5420/7420	Any Input Any Output	1.0	10.0	
SN5430/7430	Any Input Output	1.0	10.0	
SN5440/7440	Any Input Any Output	1.0	30.0	
SN7441A	B, C, or D Input A Input Any Output	1.0 2.0	N/A	
SN5442/7442	Any Input Any Output	1.0	10.0	
SN5443/7443	Any Input Any Output	1.0	10.0	
SN5444/7444	Any Input Any Output	1.0	10.0	
SN5445/7445	Any Input Any Output	1.0	12.5	
SN5446/7446	Any Input except BI/RBO BI/RBO Node Any Output except BI/RBO BI/RBO-Node	1.0 2.6	12.5 5.0	

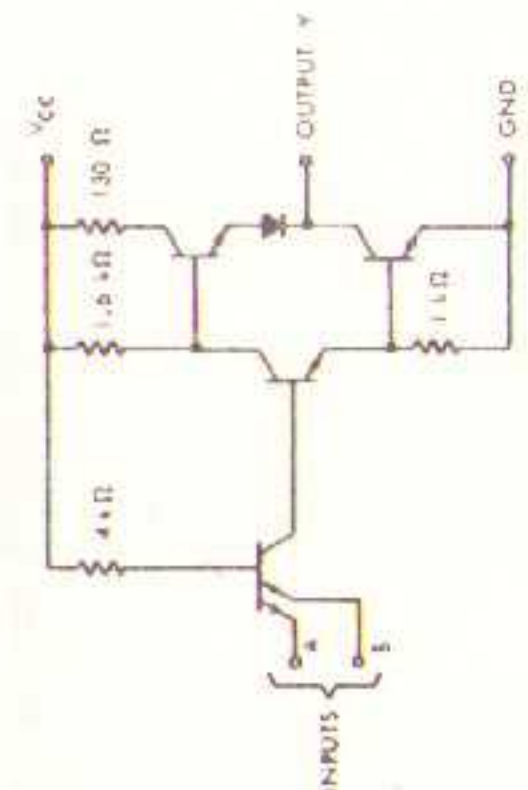
SERIES 54/74				
Device	Location	Input Load Factor	Output Load Factor	
SN5447/7447	Any Input except BI/RBO BI/RBO Node Any Output except BI/RBO BI/RBO Node	1.0 2.6	12.5 5.0	
SN5448/7448	Any Input except BI/RBO BI/RBO Node Any Output except BI/RBO BI/RBO Node	1.0 2.6	6.0 5.0	
SN5449/7449	Any Input Any Output	1.0	6.0	
SN5450/7450	A, B, C, or D Input X and Y Input Any Output	1.0 N/A	10.0	
SN5451/7451	Any Input Any Output	1.0	10.0	
SN5453/7453	A, B, C, D, E, F, G, X or Y Input Output	1.0 N/A	10.0	
SN5454/7454	Any Input Output	1.0	10.0	
SN5460/7460	Any Input X or Y Output	1.0	N/A	
SN5470/7470	J ₁ , J ₂ , J ₃ , K ₁ , K ₂ , or K ₃ Input Clock Input Preset or Clear Input Q or Q Output	1.0 1.0 2.0	10.0	
SN5472/7472	J ₁ , J ₂ , J ₃ , K ₁ , K ₂ , or K ₃ Input Clock Input Preset or Clear Input Q or Q Output	1.0 2.0 2.0	10.0	
SN5473/7473	J or K Input Clock Input Clear Input Q or Q Output	1.0 2.0 2.0	10.0	
SN5474/7474	D Input Clock Input Preset Input Clear Input Q or Q Output	1.0 2.0 2.0 3.0	10.0	

SERIES 54/74				
Device	Location	Input Load Factor	Output Load Factor	
SN5491A/7491A	A or B Input CP Input Q or Q Output	1.0 1.0	10.0	
SN5492/7492	RQ(1) or RQ(2) Input BC Input A Input Any Output	1.0 4.0 2.0	10.0	
SN5493/7493	RQ(1) or RQ(2) Input B Input A Input Any Output	1.0 2.0 2.0	10.0	
SN5494/7494	Any Input except Preset 1 or 2 Any Output	1.0 4.0	10.0	
SN5495/7495	Any Input except Mode Control Mode Control Input Any Output	1.0 2.0	10.0	
SN5496/7496	Any Input except Preset Preset Input Any Output	1.0 5.0	10.0	
SN54100/74100	Any D Input Clock 1 or Clock 2 Input Any Output	2.0 8.0	10.0	
SN54107/74107	J or K Input Clock Input Clear Input Q or Q Output	1.0 2.0 2.0	10.0	
SN54121/74121	A ₁ and A ₂ Inputs B Input Any Output	1.0 2.0	10.0	
SN54145/74145	Any Input Any Output	1.0	12.5	
SN54150/74150	Any Input Any Output: Logical 1 Logical 0	1.0	20.0 10.0	
SN54151/74151	Any Input Any Output: Logical 1 Logical 0	1.0	20.0 10.0	
SN54152/74152	Any Input Any Output: Logical 1 Logical 0	1.0	20.0 10.0	
SN54180/74180	Data Input Odd or Even Inputs Any Output: Logical 1 Logical 0	1.0 2.0	20.0 10.0	

SN7400

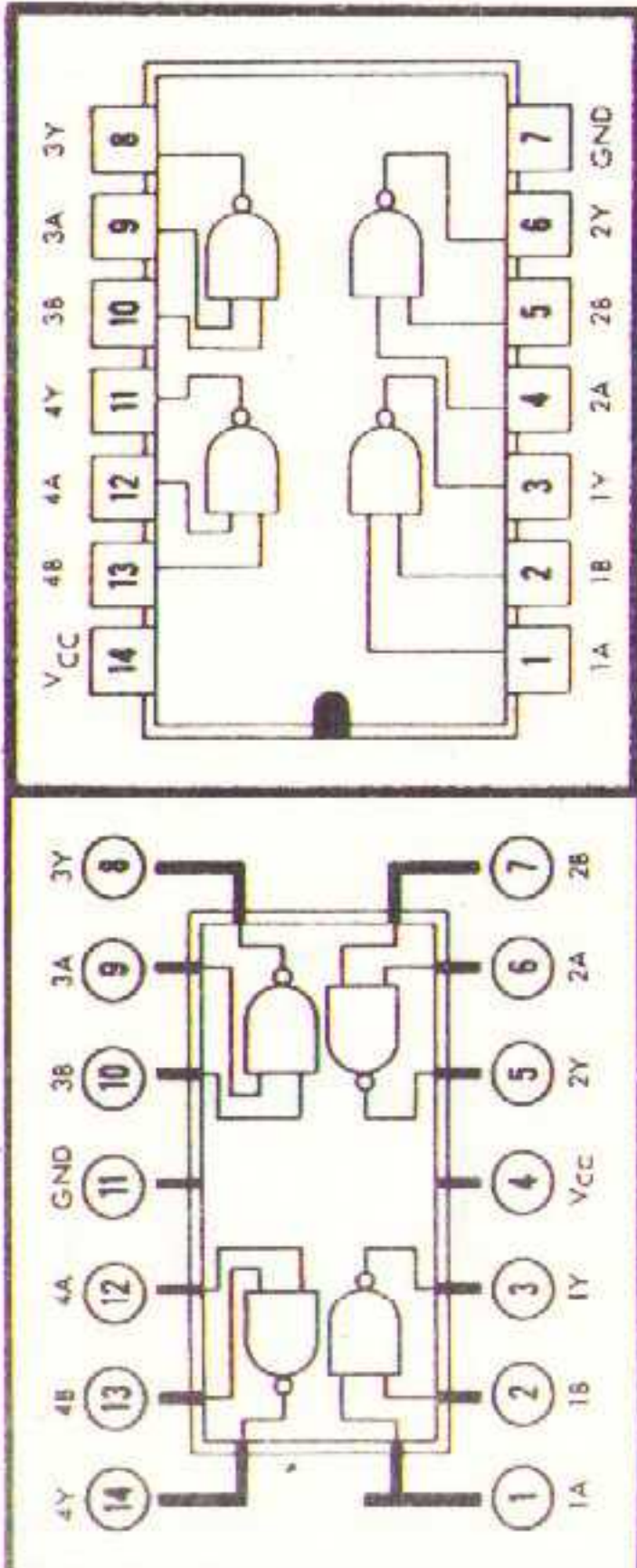
QUADRUPLE 2-INPUT POSITIVE NAND GATES

schematic (each gate)



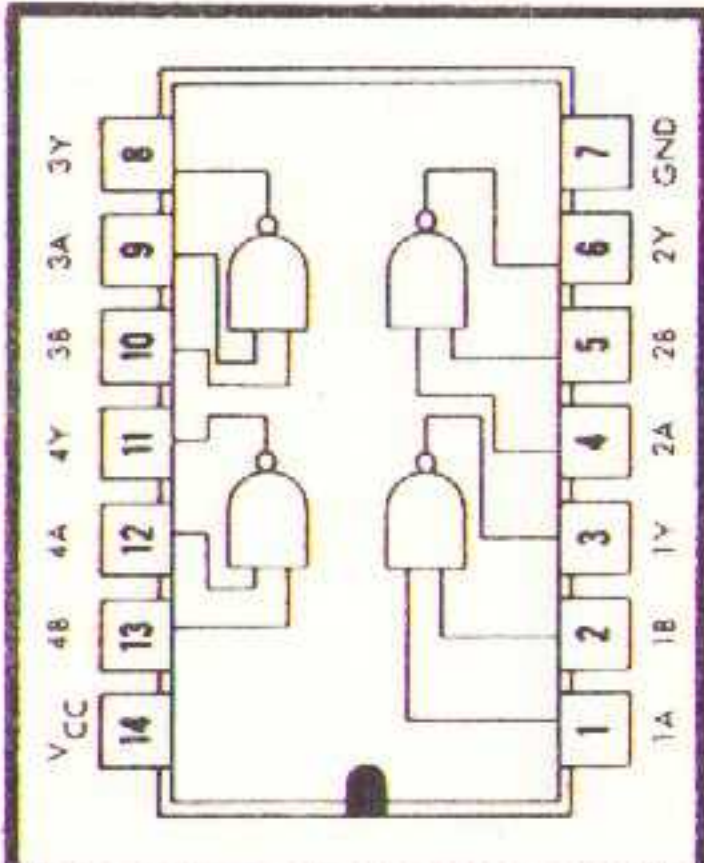
NOTE: Component values shown are nominal.

F FLAT PACKAGE
(TOP VIEW)



positive logic: $Y = AB$

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = AB$

recommended operating conditions

Supply Voltage V_{CC} : SN5400 Circuits

SN7400 Circuits

Normalized Fan-Out From Each Output, N

Operating Free-Air Temperature Range, T_A : SN5400 Circuits

SN7400 Circuits

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
-55	25	125	°C
0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2	$V_{CC} = \text{MIN}$			0.8	V
$V_{out}(1)$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$, $V_{in} = 0.8 \text{ V}$, $I_{load} = -400 \mu\text{A}$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$, $V_{in} = 2 \text{ V}$, $I_{sink} = 16 \text{ mA}$		0.22	0.4	V
$I_{in}(0)$ Logical 0 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in}(1)$ Logical 1 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$			40	μA
		$V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$			1	mA
I_{OS} Short-circuit output current§	5	$V_{CC} = \text{MAX}$	-20		-55	mA
			-18		-55	mA
$I_{CC}(0)$ Logical 0 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 5 \text{ V}$			12	mA
$I_{CC}(1)$ Logical 1 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 0$			4	mA

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		7	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		11	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

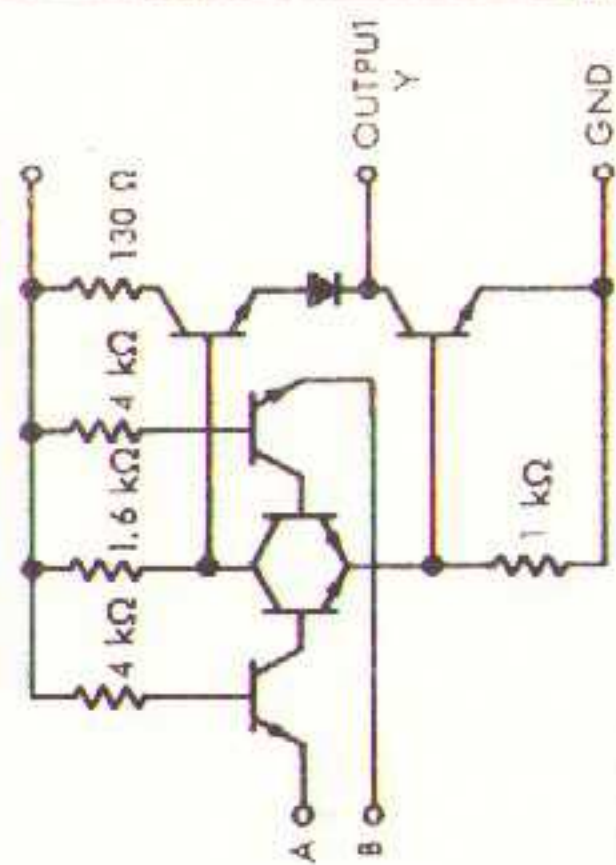
‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

SN7402

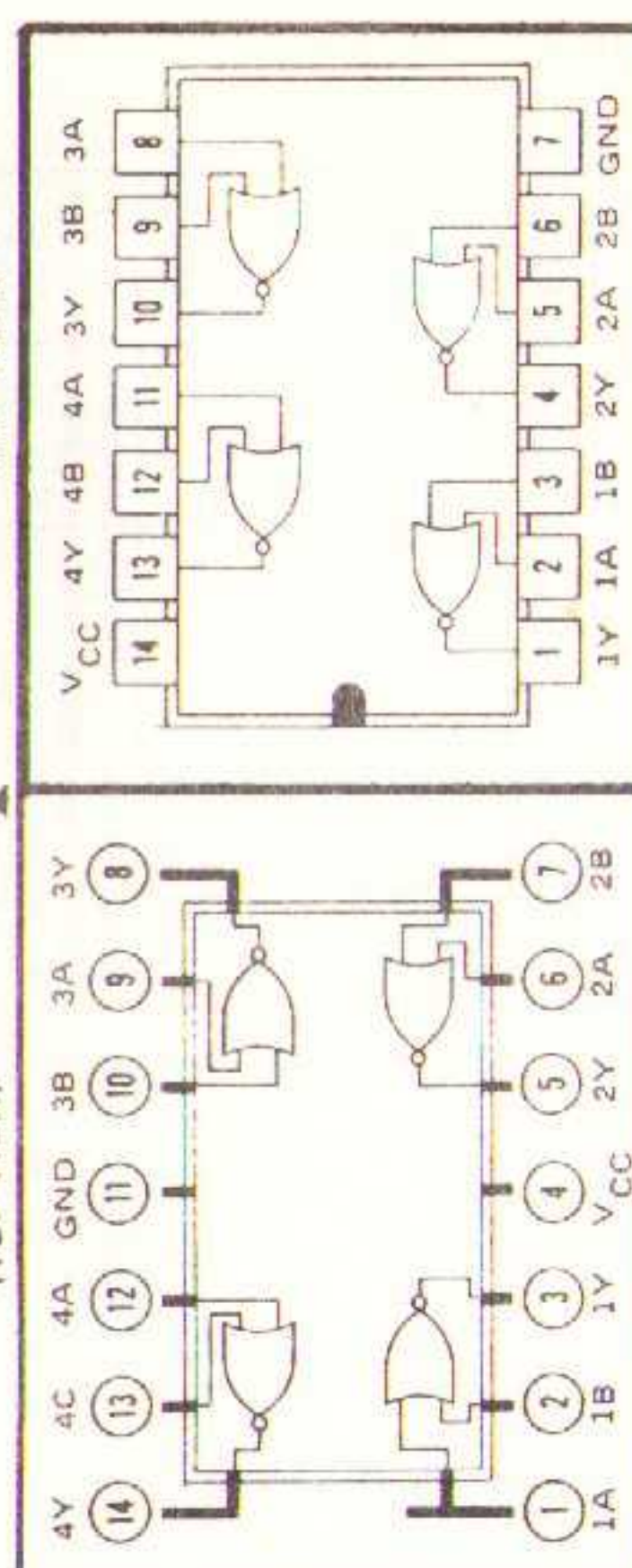
QUADRUPLE 2-INPUT POSITIVE NOR GATES

schematic (each gate)



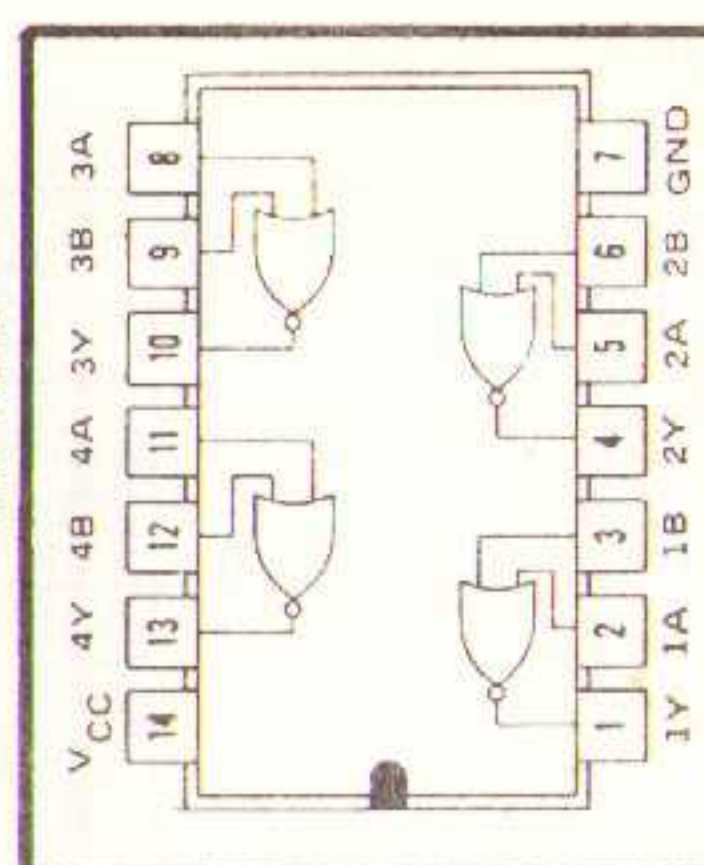
NOTE: Component values shown are nominal.

S FLAT PACKAGE
(TOP VIEW)



positive logic: $Y = A + B$

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = A + B$

recommended operating conditions

Supply Voltage V_{CC} : SN5402 Circuits

SN7402 Circuits

Normalized Fan-Out From Each Output, N

Operating Free-Air Temperature Range, T_A : SN5402 Circuits

SN7402 Circuits

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
-55	25	125	°C
0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	8	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	9	$V_{CC} = \text{MIN}$			0.8	V
$V_{out}(1)$ Logical 1 output voltage	9	$V_{CC} = \text{MIN}$, $V_{in} = 0.8 \text{ V}$, $I_{load} = -400 \mu\text{A}$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	10	$V_{CC} = \text{MIN}$, $V_{in} = 2 \text{ V}$, $I_{sink} = 16 \text{ mA}$		0.22	0.4	V
$I_{in}(0)$ Logical 0 level input current (each input)	11	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in}(1)$ Logical 1 level input current (each input)	12	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$			40	μA
		$V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$			1	mA
I_{OS} Short-circuit output current§	13	$V_{CC} = \text{MAX}$	-20		-55	mA
			-18		-55	mA
$I_{CC}(0)$ Logical 0 level supply current	14	$V_{CC} = \text{MAX}$, $V_{in} = 5 \text{ V}$			14	mA
$I_{CC}(1)$ Logical 1 level supply current	14	$V_{CC} = \text{MAX}$, $V_{in} = 0$			8	mA

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		8	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

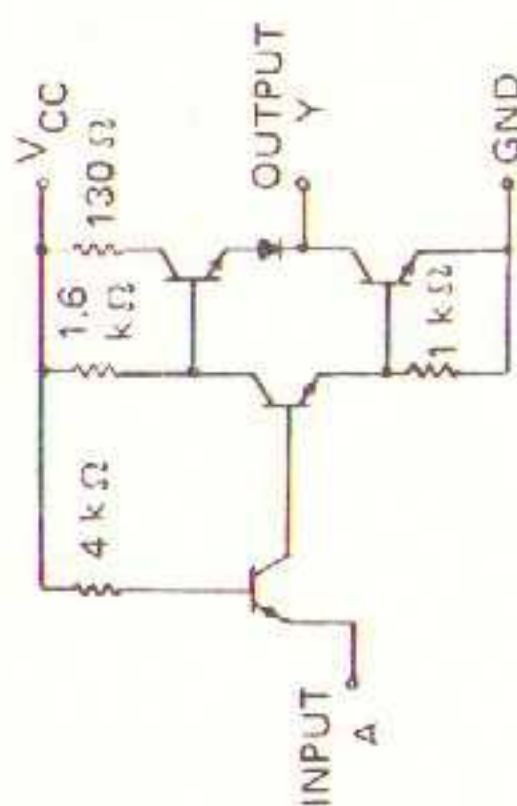
‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

SN7404

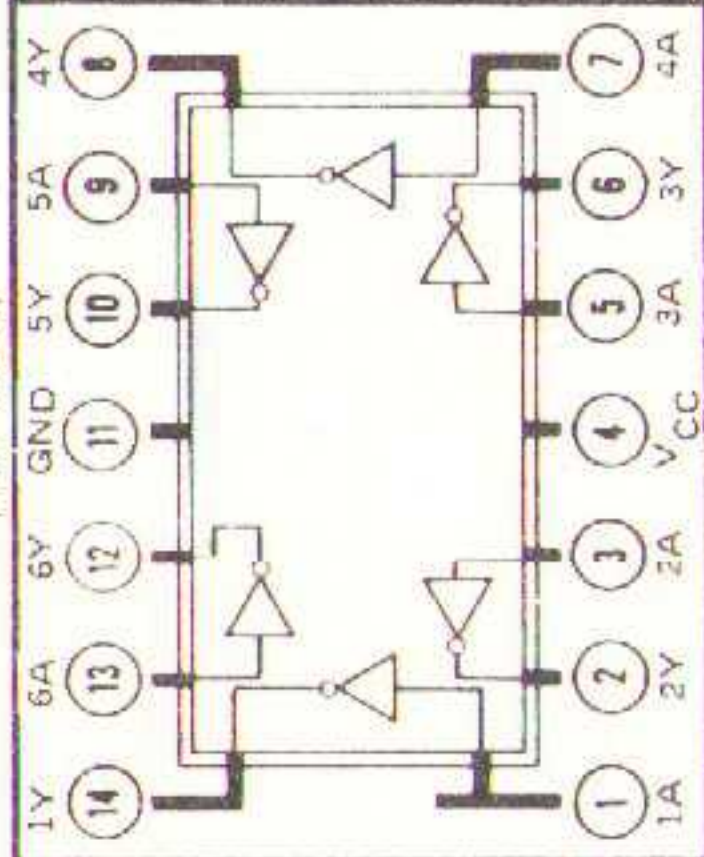
HEX INVERTERS

schematic (each inverter)



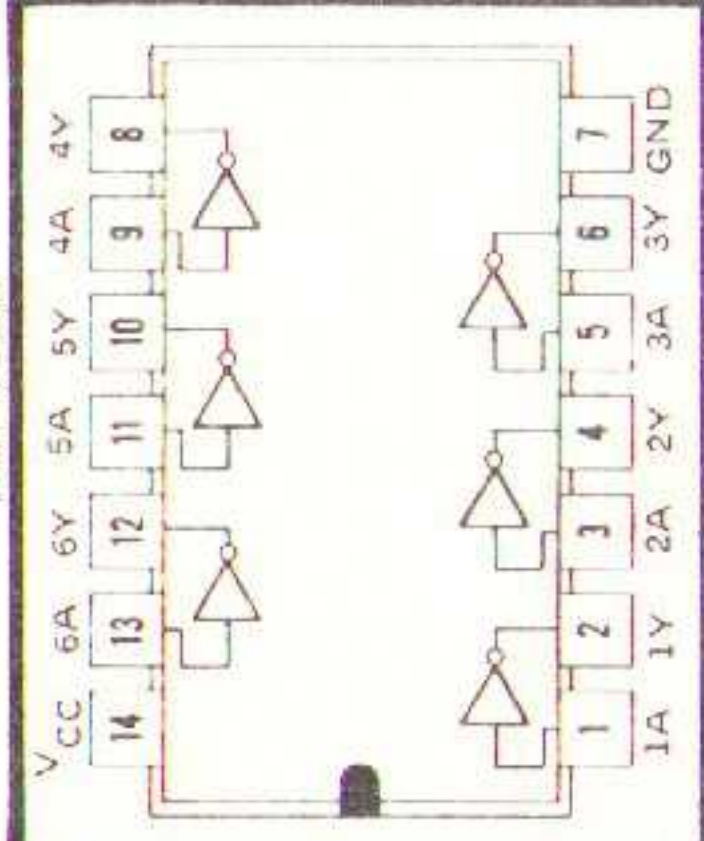
NOTE: Component values shown are nominal

S FLAT PACKAGE
(TOP VIEW)



positive logic: $Y = \bar{A}$

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



recommended operating conditions

Supply Voltage V_{CC} : SN5404 Circuits
SN7404 Circuits
Normalized Fan-Out From Each Output, N
Operating Free-Air Temperature Range, T_A : SN5404 Circuits
SN7404 Circuits

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
-55	25	125	$^{\circ}\text{C}$
0	25	70	$^{\circ}\text{C}$

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at input terminal to ensure logical 0 level at output	15	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	15	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	16	$V_{CC} = \text{MIN}$, $V_{in} = 0.8\text{ V}$, $I_{load} = -400\text{ }\mu\text{A}$	2.4	3.3		V
$V_{out(0)}$ Logical 0 output voltage	15	$V_{CC} = \text{MIN}$, $V_{in} = 2\text{ V}$, $I_{sink} = 16\text{ mA}$		0.22	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	17	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current	18	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{ V}$, $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{ V}$			40	μA
I_{OS} Short-circuit output current§	19	$V_{CC} = \text{MAX}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current	20	$V_{CC} = \text{MAX}$, $V_{in} = 5\text{ V}$	-18		-55	mA
$I_{CC(1)}$ Logical 1 level supply current	20	$V_{CC} = \text{MAX}$, $V_{in} = 0$		18	33	mA

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$, $N = 10$

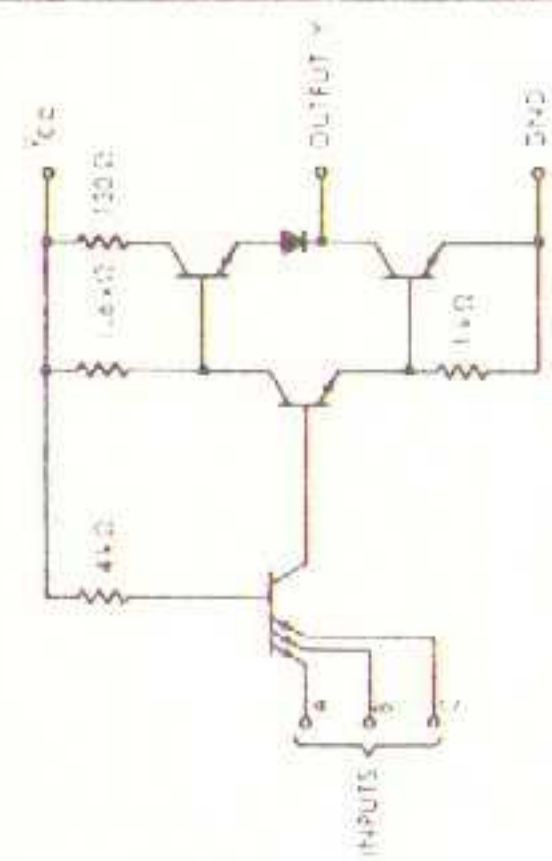
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		8	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.
§ Not more than one output should be shorted at a time.

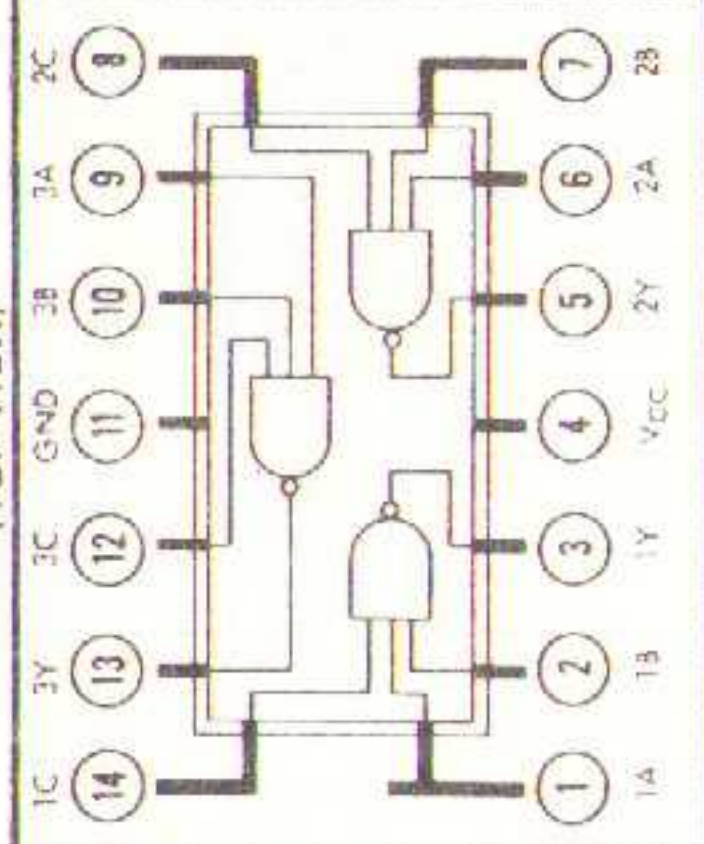
SN7410

TRIPLE 3-INPUT POSITIVE NAND GATES

schematic (each gate)

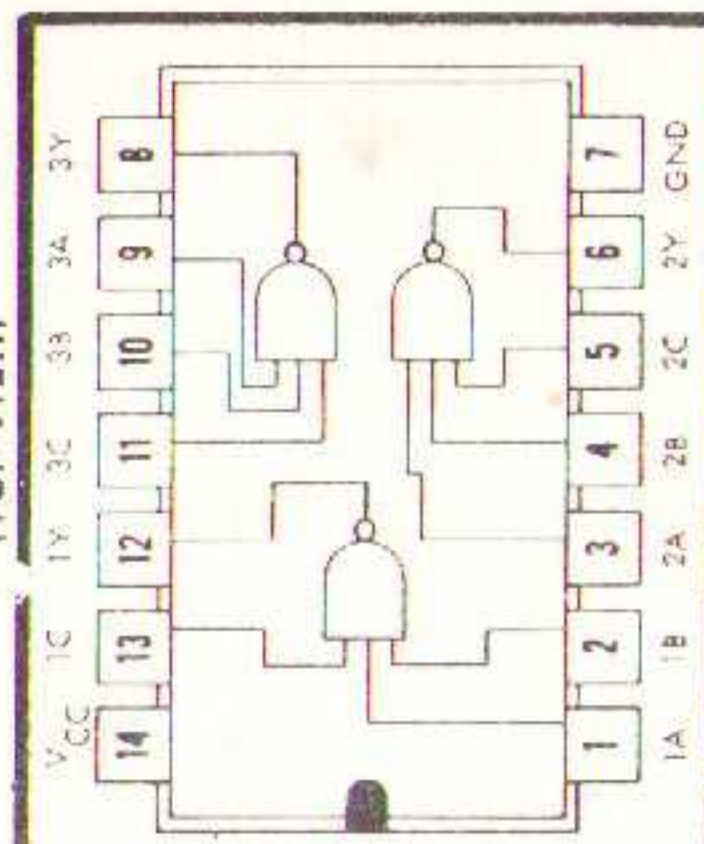


S FLAT PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABC}$

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NOTE: Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} : SN5410 Circuits
SN7410 Circuits
Normalized Fan-Out From Each Output, N
Operating Free-Air Temperature Range, T_A : SN5410 Circuits
SN7410 Circuits

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
-55	25	125	$^{\circ}\text{C}$
0	25	70	$^{\circ}\text{C}$

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$, $V_{in} = 0.8\text{ V}$, $I_{load} = -400\text{ }\mu\text{A}$	2.4	3.3		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$, $V_{in} = 2\text{ V}$, $I_{sink} = 16\text{ mA}$		0.22	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{ V}$, $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{ V}$			40	μA
I_{OS} Short circuit output current§	5	$V_{CC} = 5.5\text{ V}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 5\text{ V}$	-18		-55	mA
$I_{CC(1)}$ Logical 1 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 0$		9	16.5	mA

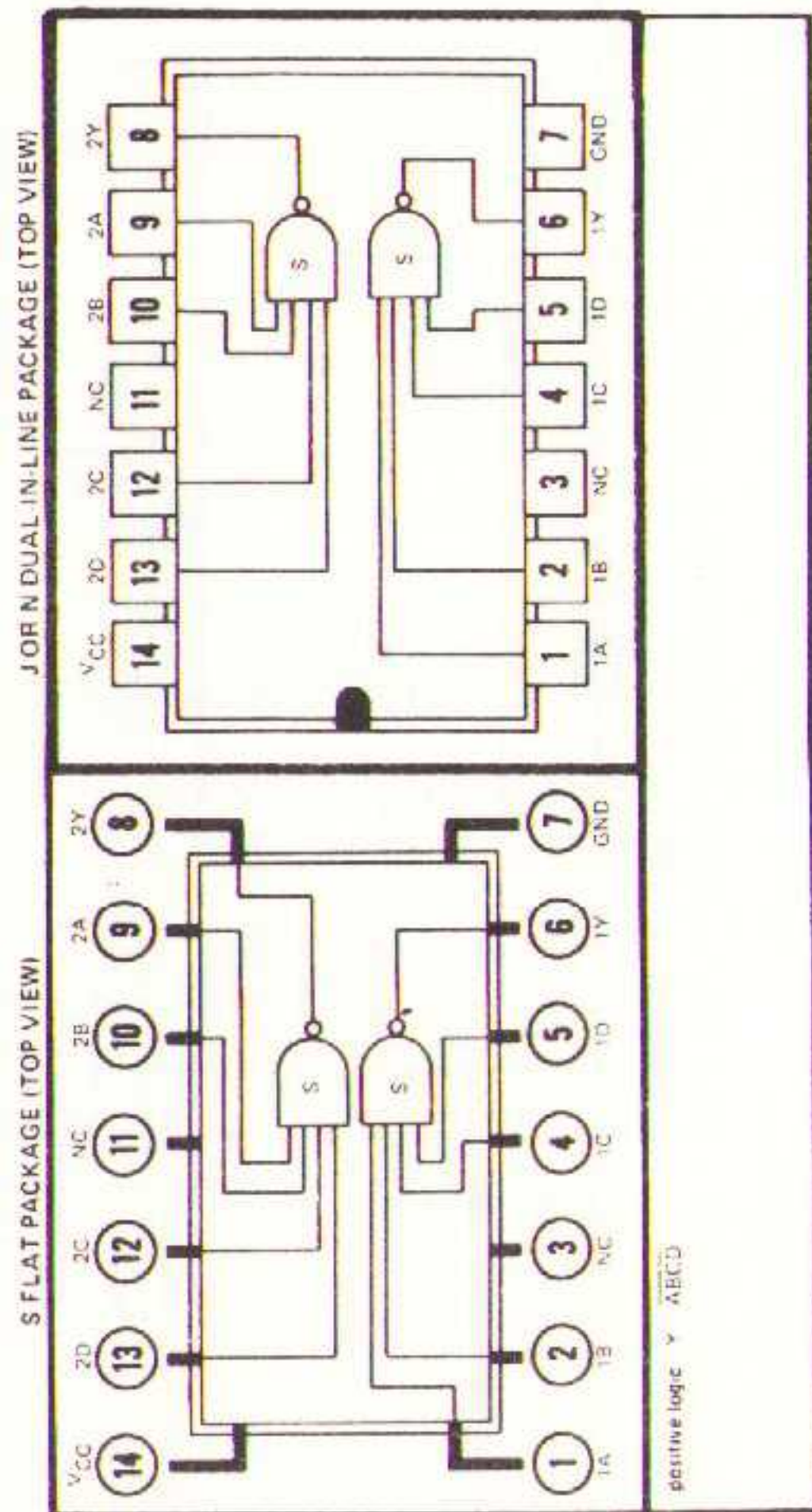
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		7	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		11	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.
§ Not more than one output should be shorted at a time.

SN7413

DUAL 4-INPUT SCHMITT-TRIGGERED POSITIVE NAND GATES



features

- stable operation from very slow input ramps
- threshold levels temperature compensated — use for accurate circuit delays
- very high noise immunity plus regenerative action produces ideal pulse shaper
- 0.8 volt temperature compensated hysteresis
- inputs and outputs TTL and DTL compatible
- typical propagation delay time — 17 nanoseconds
- typical power dissipation — 85 milliwatts total

description

The SN5413 SN7413 dual Schmitt-trigger consists of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically each circuit functions as a four input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive and negative going signals. The hysteresis, or backlash, which is the difference between the two threshold levels is typically 800 millivolts.

An important design feature is the built in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically the hysteresis changes by less than 0.3 mV/°C over -55°C to +125°C, and over the 0°C to 70°C range it is virtually unchanged.

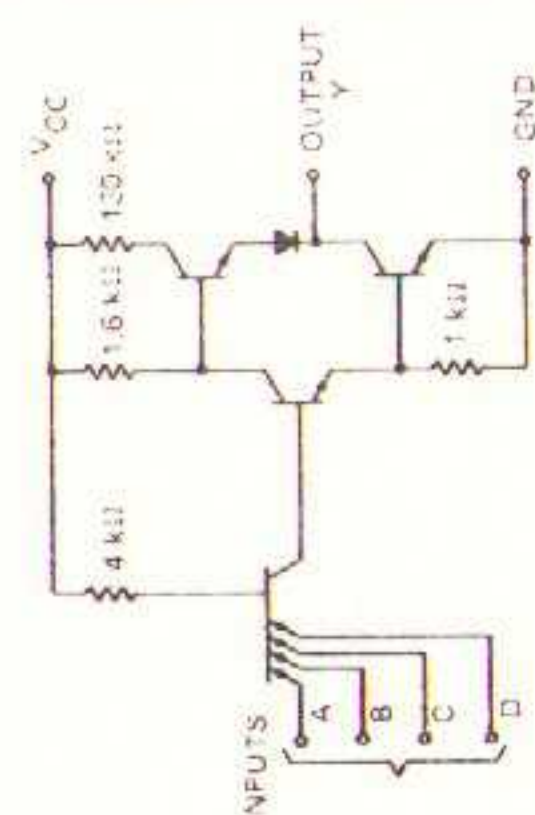
The Schmitt will trigger from very slow input ramps producing stable output signal. It can also be triggered from straight dc levels.

These circuits are completely compatible with all popular TTL or DTL families. Typical average power dissipation is 42.5 milliwatts per gate, and average propagation delay times is 17 nanoseconds typically. The SN5413 is characterized for operation over the full military temperature range of -55°C to 125°C, and the SN7413 is characterized for operation from 0°C to 70°C.

SN7420

DUAL 4-INPUT POSITIVE NAND GATES

schematic (each gate)



Component values shown are nominal.
NC—No Internal Connection

positive logic: Y = ABCD

recommended operating conditions

Supply Voltage V_{CC} : SN5420 Circuits
SN7420 Circuits
Normalized Fan-Out From Each Output, N: 10
Operating Free-Air Temperature Range, T_A : SN5420 Circuits
SN7420 Circuits

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
-55	25	125	°C
0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = \text{MIN}$		0.8		V
$V_{out}(1)$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$, $I_{load} = -400 \mu A$, $V_{in} = 0.8 V$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$, $I_{sink} = 16 \text{ mA}$, $V_{in} = 2 V$		0.22	0.4	V
$I_{in}(0)$ Logical 0 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 V$		-1.6		mA
$I_{in}(1)$ Logical 1 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 V$		40		μA
I_{OS} Short-circuit output current§	5	$V_{CC} = \text{MAX}$, $V_{in} = 5.5 V$		1		mA
$I_{CC}(0)$ Logical 0 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 5 V$		6	11	mA
$I_{CC}(1)$ Logical 1 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 0$		2	4	mA

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		8	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

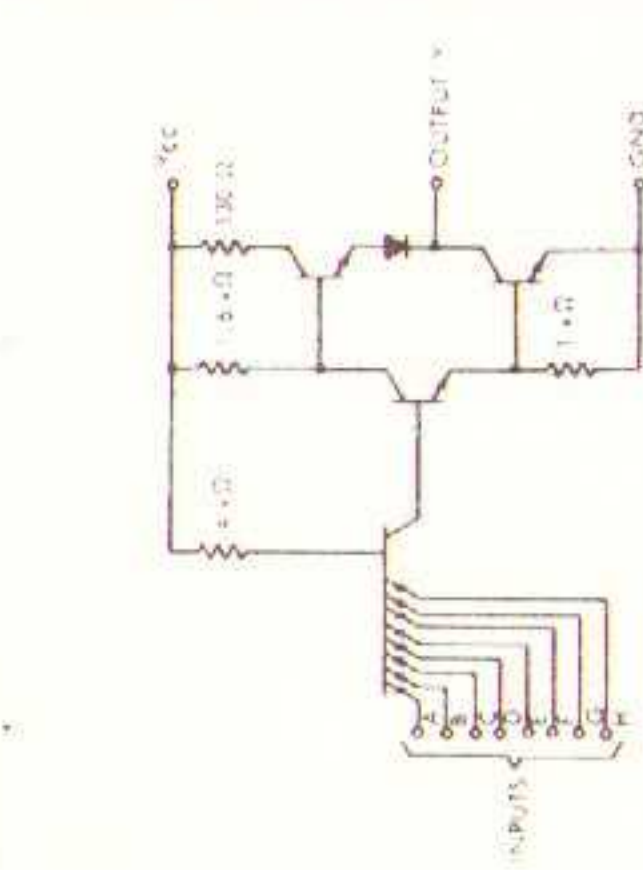
‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

§ Not more than one output shr shorted at a time.

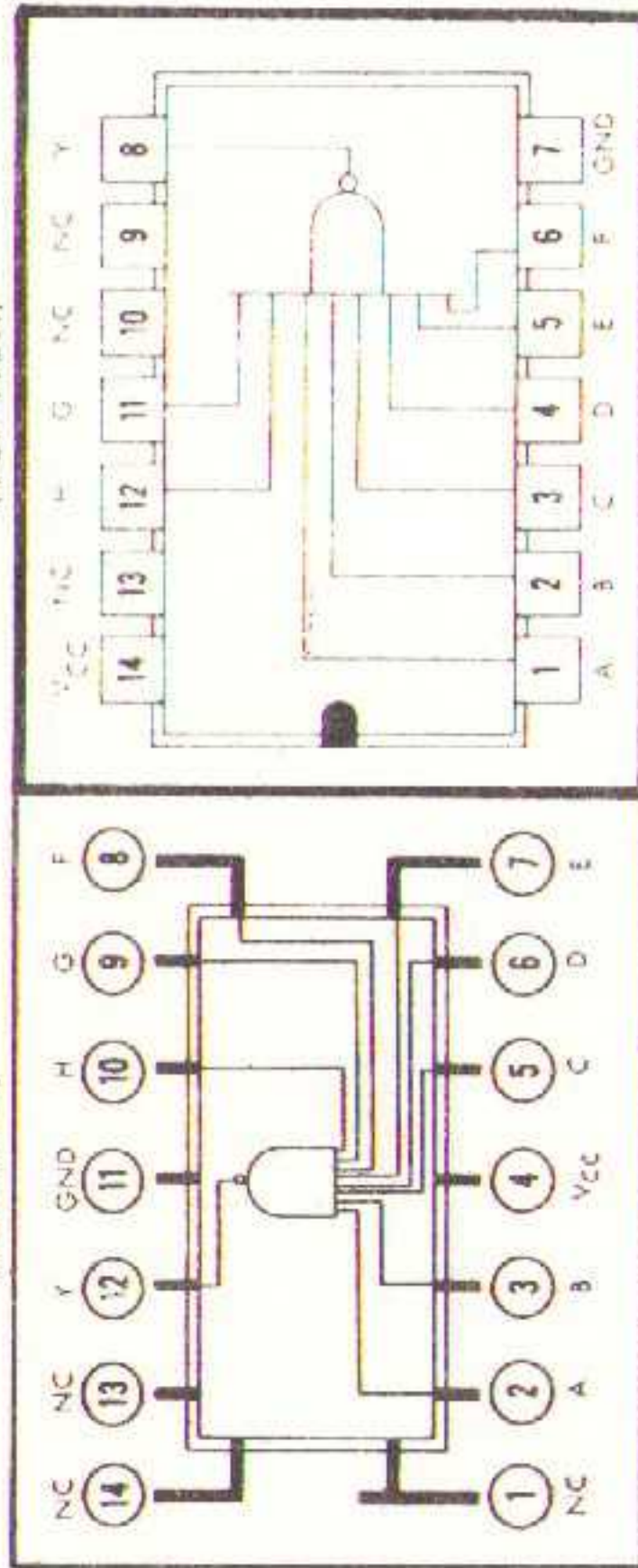
SN7430

8-INPUT POSITIVE NAND GATES

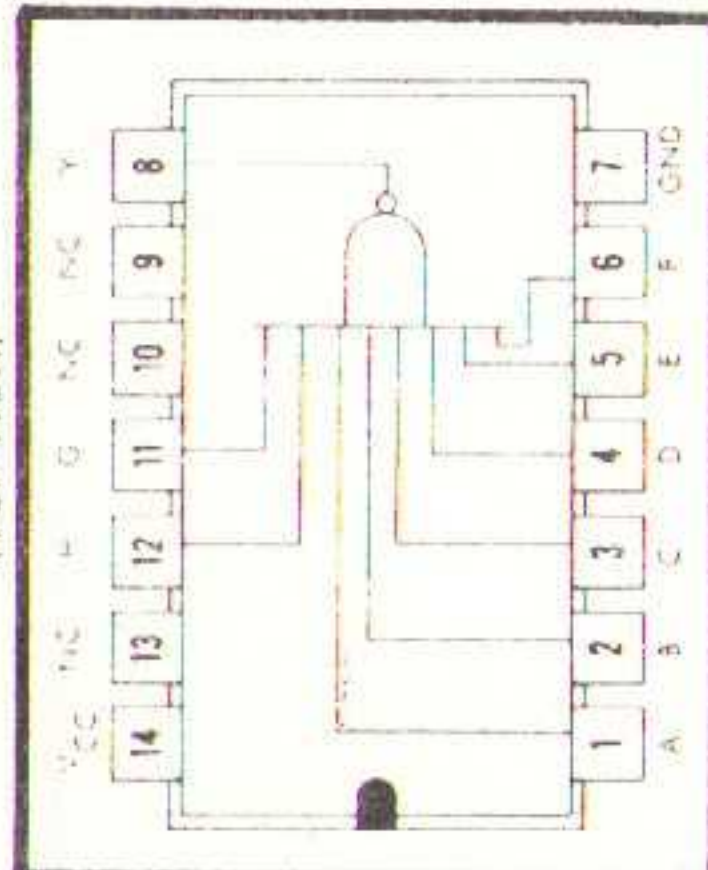
schematic



S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



Component values shown are nominal.
NC—No Internal Connection

recommended operating conditions

Supply Voltage V_{CC} :	SN5430 Circuits	MIN	NOM	MAX	UNIT
	SN7430 Circuits	4.5	5	5.5	V
Normalized Fan-Out From Output, N :		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A :		-55	25	125	°C
	SN5430 Circuits	0	25	70	°C
	SN7430 Circuits				

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = \text{MIN}$		0.8		V
$V_{out}(1)$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$, $V_{in} = 0.8 \text{ V}$, $I_{load} = -400 \mu\text{A}$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$, $V_{in} = 2 \text{ V}$, $I_{sink} = 16 \text{ mA}$		0.22	0.4	V
$I_{in}(0)$ Logical 0 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$		-1.6		mA
$I_{in}(1)$ Logical 1 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$		40		μA
I_{OS} Short-circuit output current [‡]	5	$V_{CC} = \text{MAX}$	SN5430 -20 SN7430 -18	-55		mA
$I_{CC}(0)$ Logical 0 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 5 \text{ V}$		3	6	mA
$I_{CC}(1)$ Logical 1 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 0$		1	2	mA

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

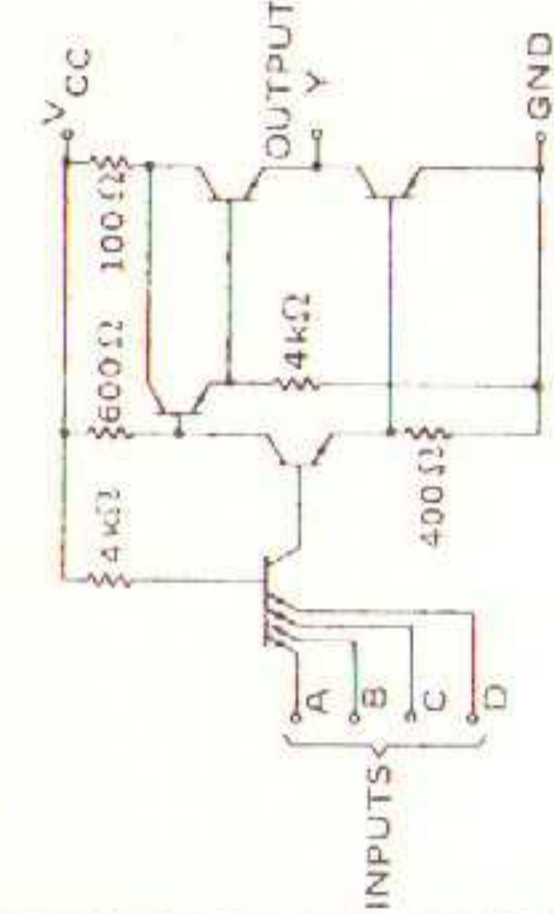
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		8	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		13	22	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
[§] Not more than one output should be shorted at a time.

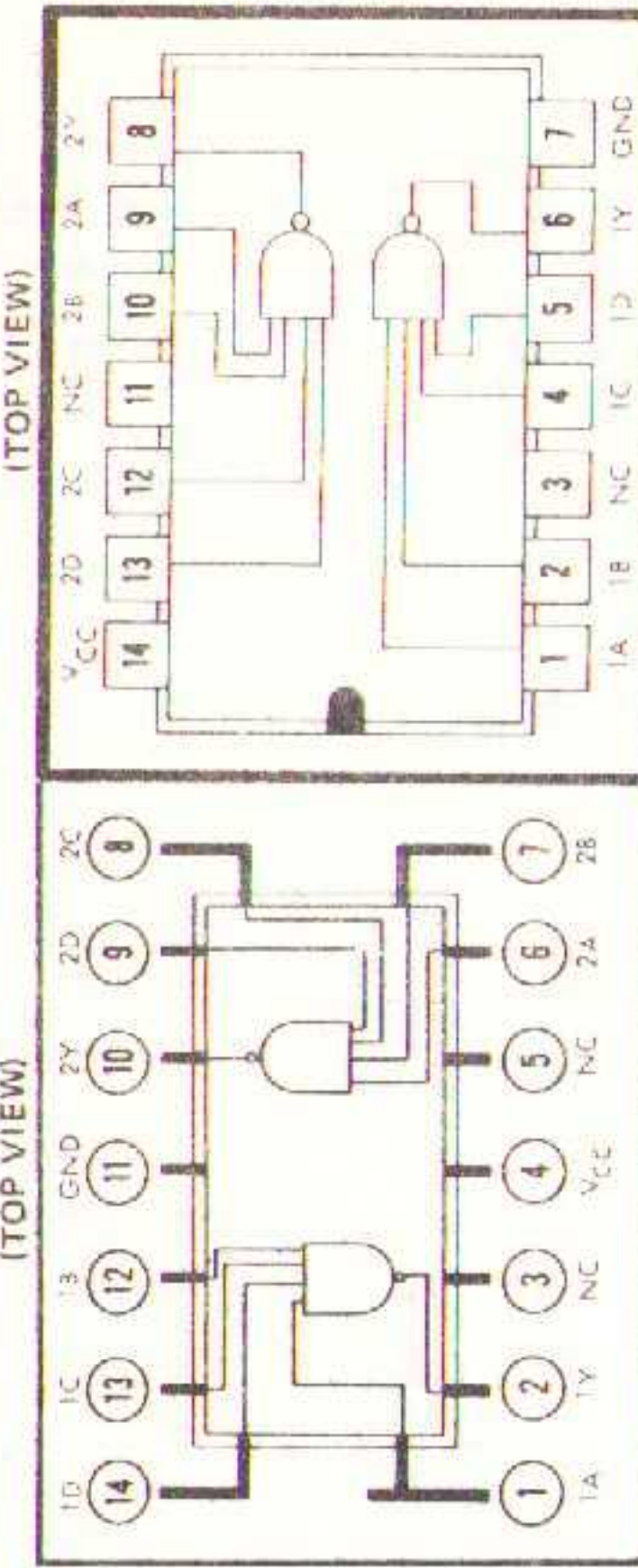
SN7440

DUAL 4-INPUT POSITIVE NAND BUFFERS

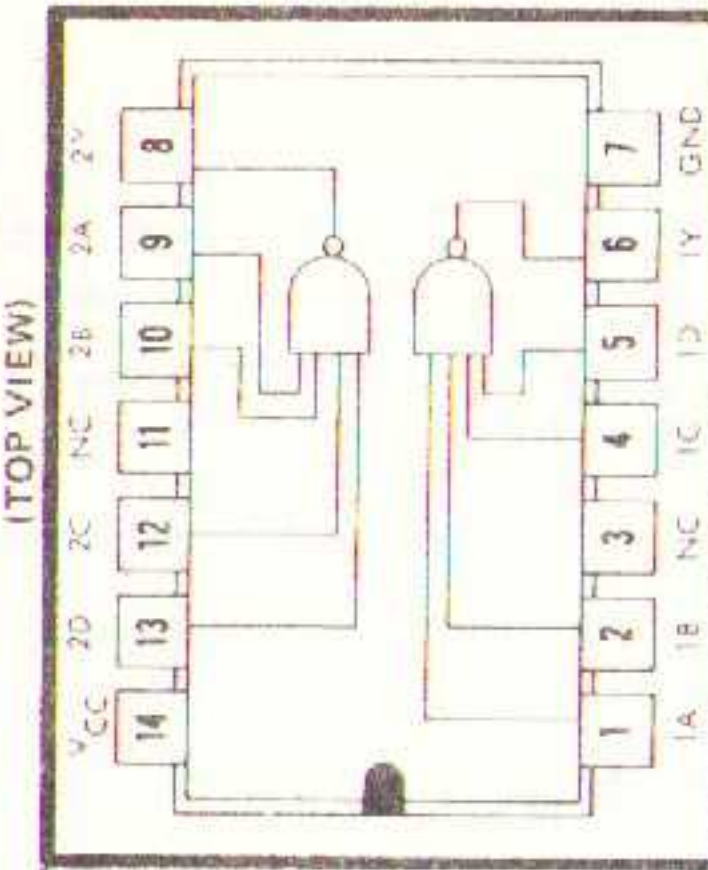
schematic (each gate)



S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



Component values shown are nominal.
NC—No Internal Connection

recommended operating conditions

Supply Voltage V_{CC} :	SN5440 Circuits	MIN	NOM	MAX	UNIT
	SN7440 Circuits	4.5	5	5.5	V
Normalized Fan-Out From Output, N :		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A :		-55	25	125	°C
	SN5440 Circuits	0	25	70	°C
	SN7440 Circuits				

electrical characteristics (over recommended free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = \text{MIN}$		0.8		V
$V_{out}(1)$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$, $V_{in} = 0.8 \text{ V}$, $I_{load} = -1.2 \text{ mA}$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$, $V_{in} = 2 \text{ V}$, $I_{sink} = 48 \text{ mA}$		0.28	0.4	V
$I_{in}(0)$ Logical 0 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$		-1.6		mA
$I_{in}(1)$ Logical 1 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$		40		μA
I_{OS} Short-circuit output current [‡]	5	$V_{CC} = \text{MAX}$	SN5440 -20 SN7440 -18	-70		mA
$I_{CC}(0)$ Logical 0 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 5 \text{ V}$		17	27	mA
$I_{CC}(1)$ Logical 1 level supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 0$		2	4	mA

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 30$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15 \text{ pF}$, $R_L = 133 \Omega$		8	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15 \text{ pF}$, $R_L = 133 \Omega$		13	22	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
[§] Not more than one output should be shorted at a time.

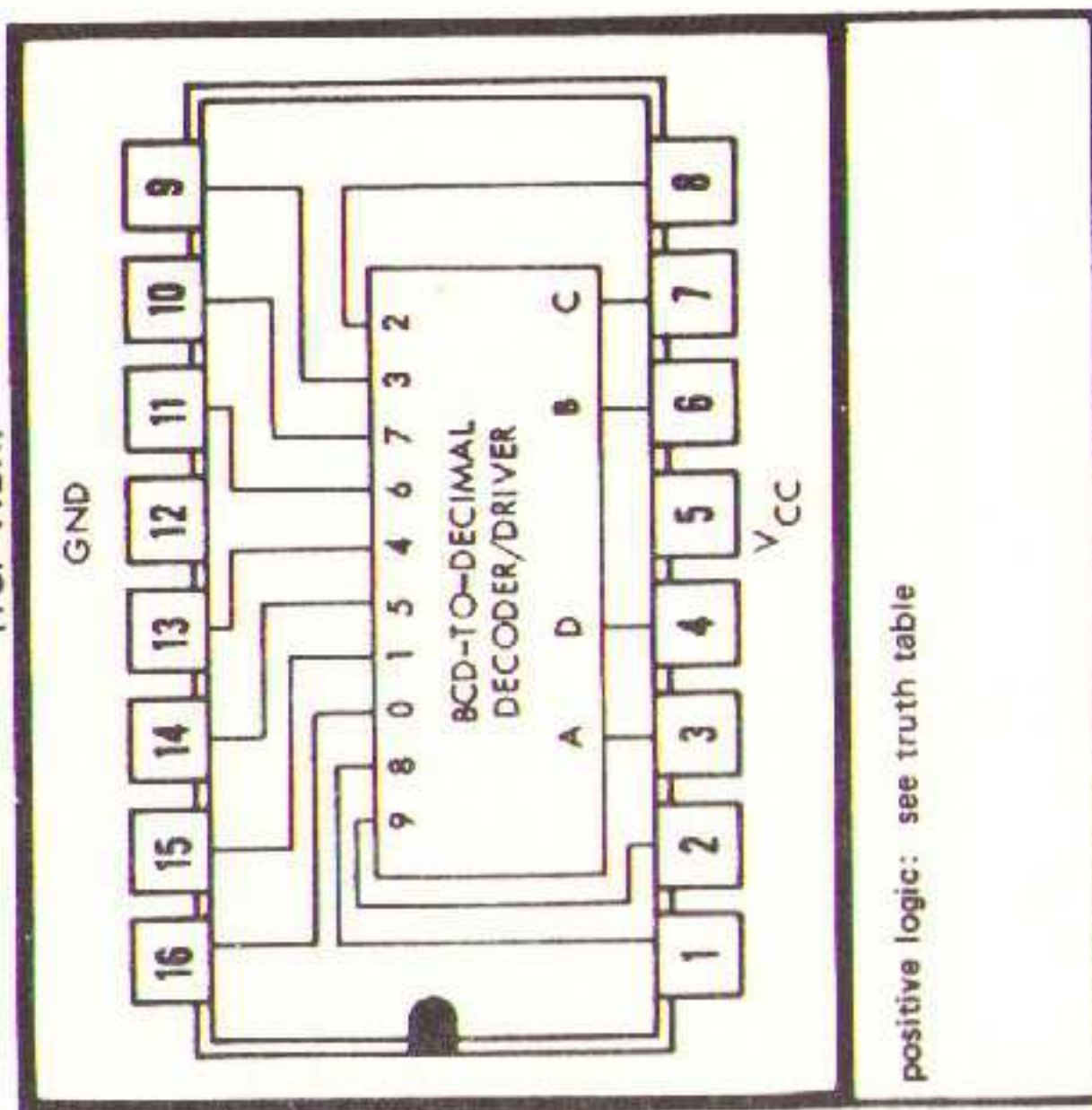
SN7441A

BCD-TO-DECIMAL DECODER/DRIVER

A SERIES 74 BCD-TO-DECIMAL DECODER

For Driving Gas-Filled Cold-Cathode Indicator Tubes

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see truth table

TRUTH TABLE

logic	INPUT				OUTPUT ON:
	D	C	B	A	
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9

description

The SN7441A is a monolithic, BCD-to-decimal decoder incorporating high performance output transistors designed for driving gas-filled, cold-cathode indicator tubes. The BCD-to-decimal decoder consists of familiar transistor-transistor-logic (TTL) gate circuits which select one of the ten decimal output drivers. The BCD inputs are fully compatible with Series 74 logic outputs; and, in addition, physical placement of these inputs is coincidental with the BCD output of the SN7490 decade counter. The ten high-breakdown, n-p-n transistors have a maximum reverse current of 50 μ A at 55 V over the operating temperature range.

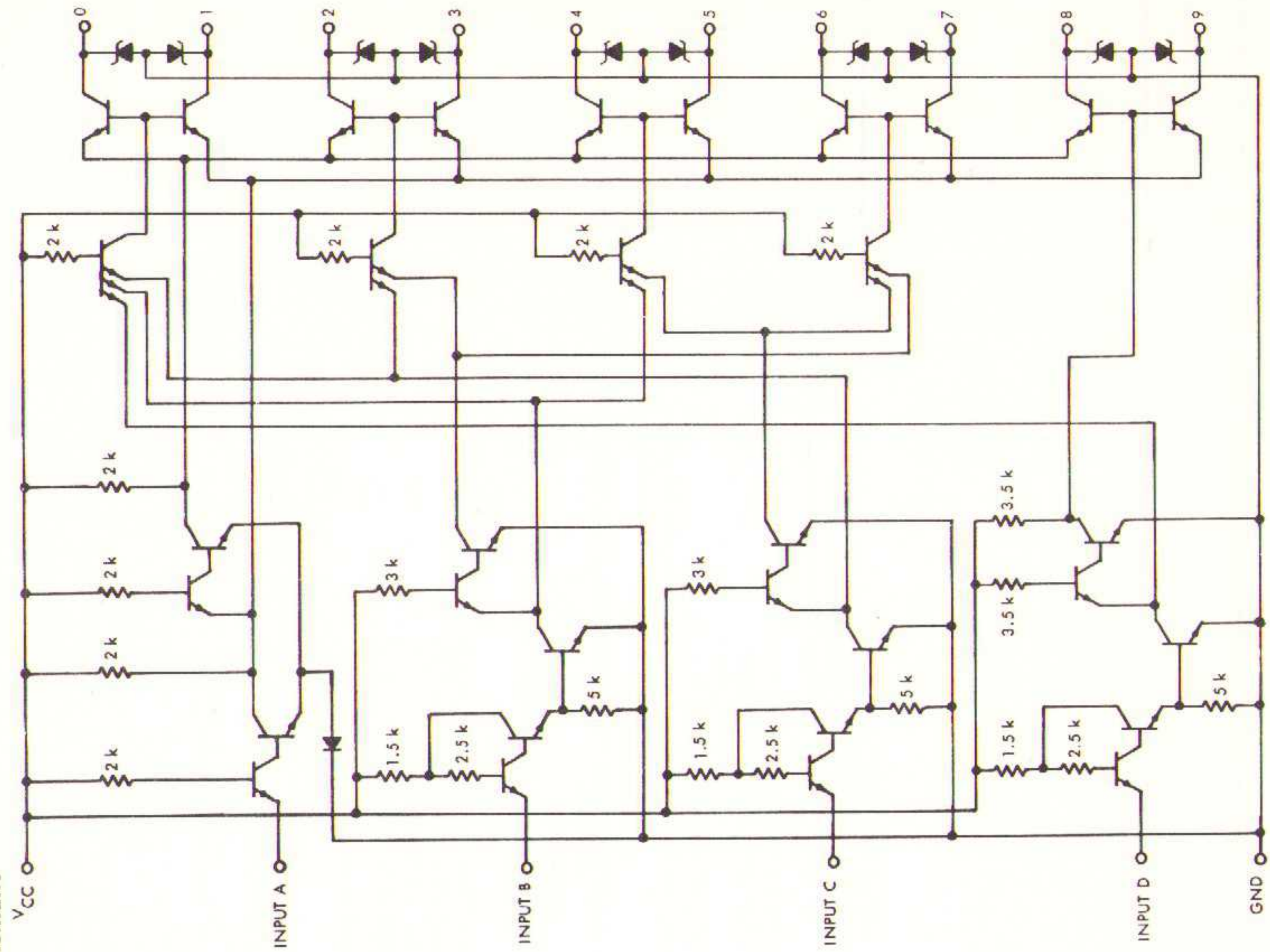
A typical application shows the SN7441A used as a gas-filled, display-indicator driver.

recommended operating conditions

Supply Voltage V_{CC} (See Note 1)	4.75 V to 5.25 V
Maximum Voltage on any Output	70 V
absolute maximum ratings (over operating temperature range unless otherwise noted)	
Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Current into any Output (Off-State)	2 mA
Operating Free-Air Temperature Range:	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

- NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

schematic



Component values shown are nominal.
All resistor values are in ohms.

electrical characteristics, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted.

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
$V_{in(1)}$	1	$V_{CC} = 4.75\text{ V}$	2			V
$V_{in(0)}$	1	$V_{CC} = 4.75\text{ V}$			0.8	V
V_{on}	1	$V_{CC} = 4.75\text{ V}, I_{on} = 7\text{ mA}$			2.5	V
I_{off}	2	$V_{CC} = 5.25\text{ V}, V_{out} = 55\text{ V}$ $V_{CC} = 5.25\text{ V}, V_{out} = 70\text{ V}$			50	μA
$I_{in(1)}$	3	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$ $V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			40	μA
$I_{in(1)}$	3	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$ $V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			80	μA
$I_{in(1)}$	3	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$ $V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(0)}$	4	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$	4	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-3.2	mA
I_{CC}	3	$V_{CC} = 5.25\text{ V}$		21	42	mA

[†] This typical value is at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

typical application data

The SN7441A output transistors are capable of withstanding voltages and sinking current required to operate most types of gas-filled indicator tubes.

Clamping diodes have been incorporated in the outputs of this improved decoder/driver.

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

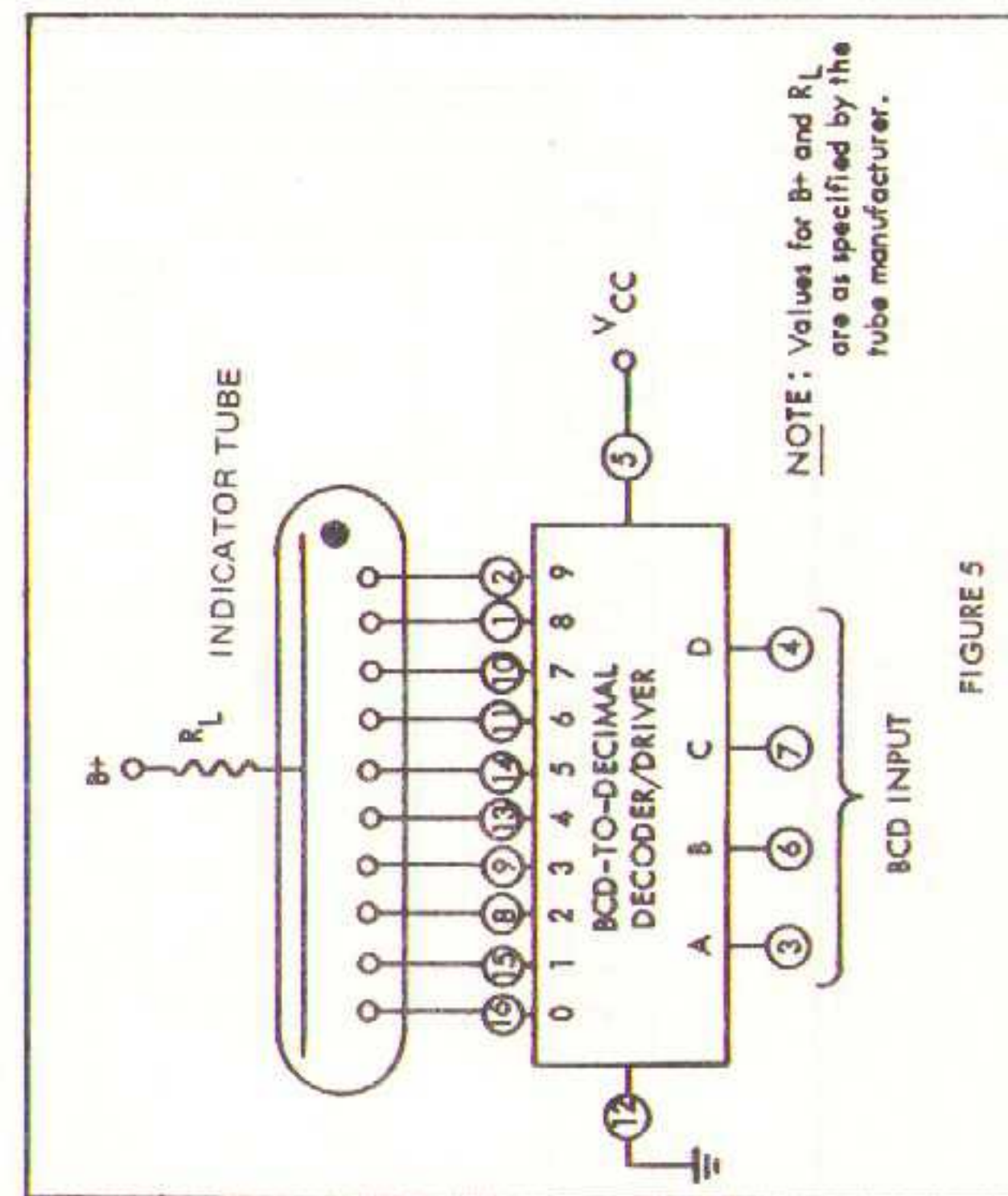


FIGURE 5

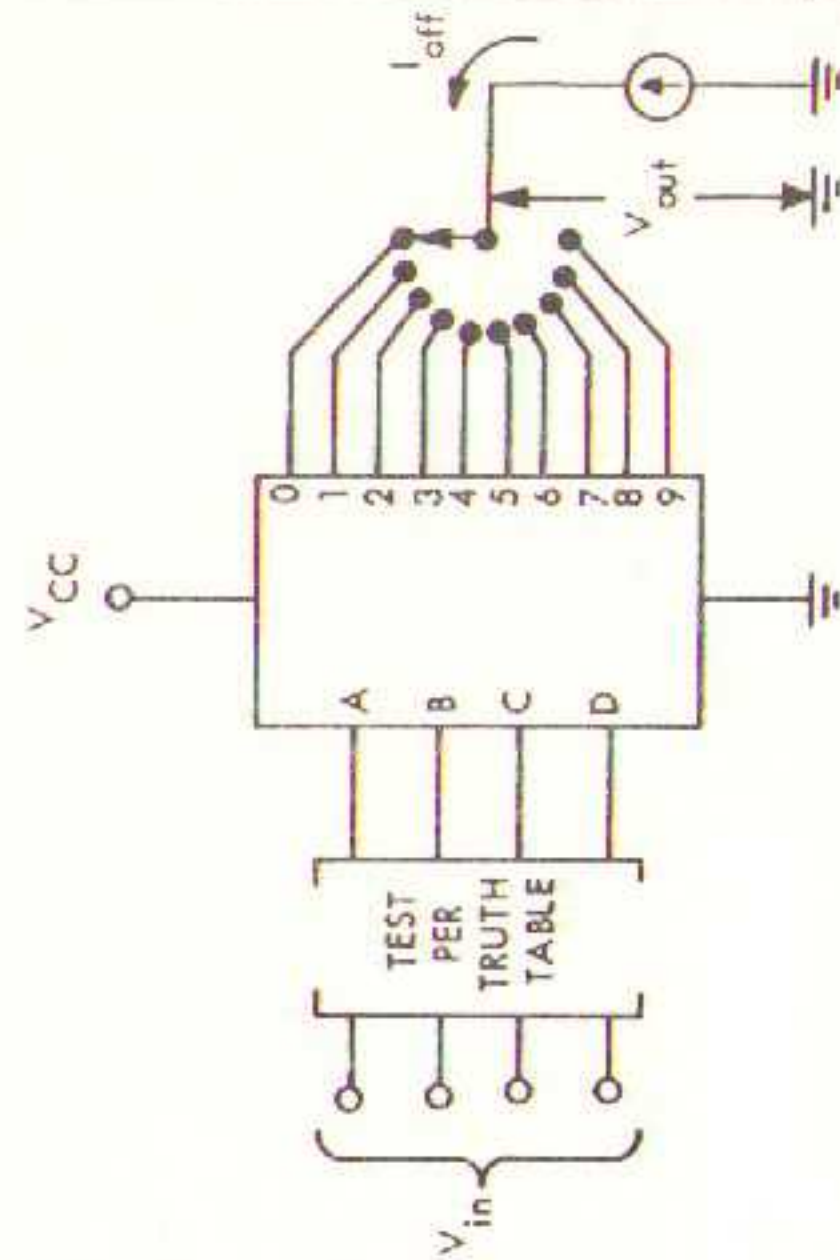


FIGURE 2

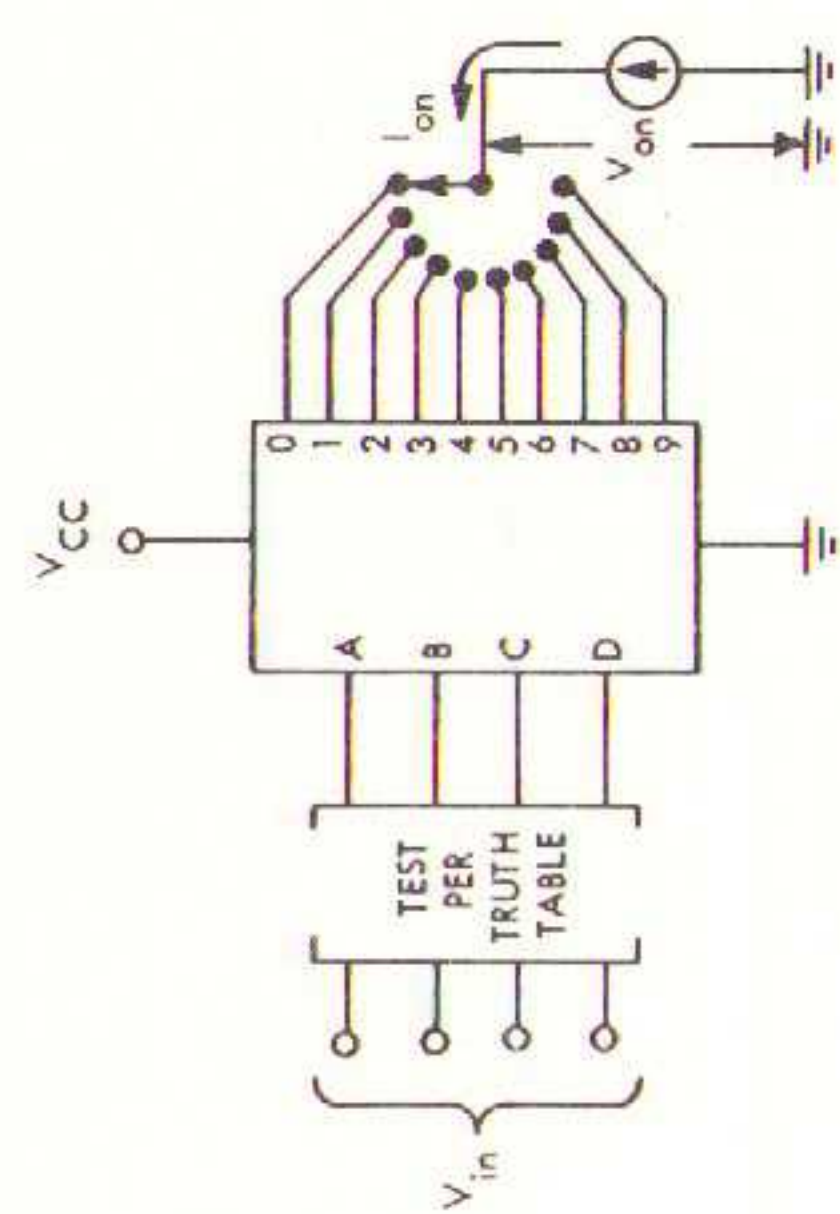


FIGURE 1

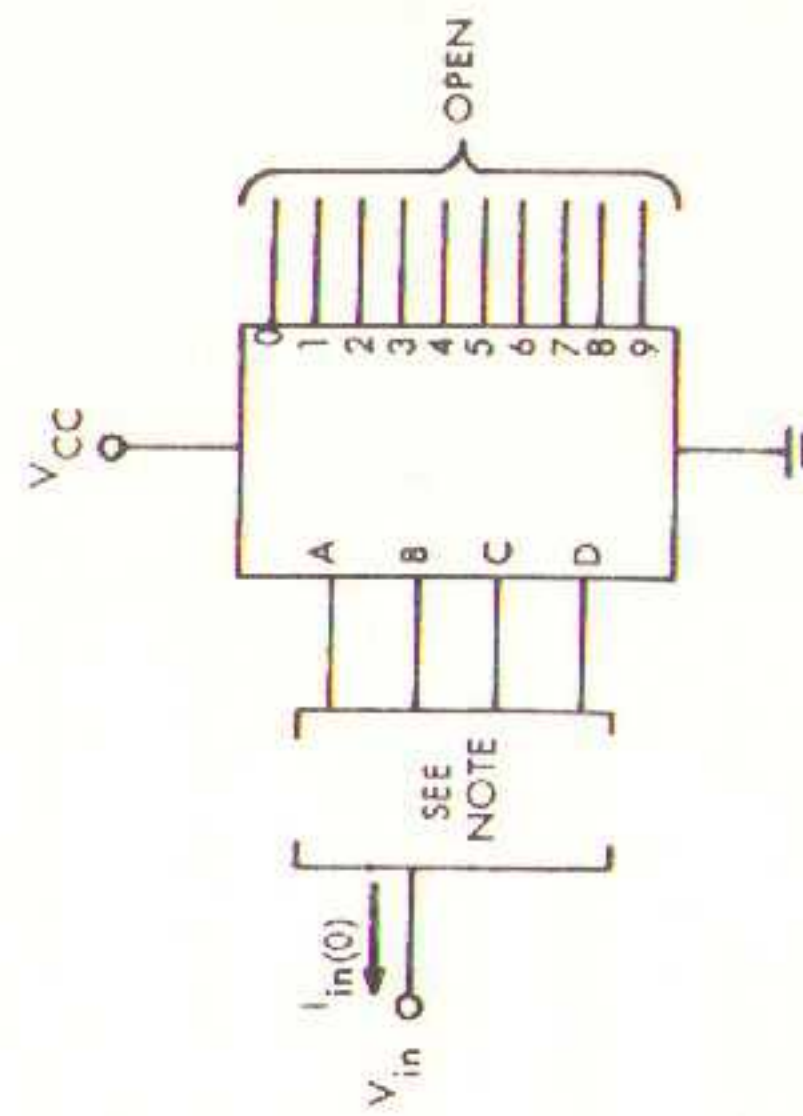


FIGURE 4

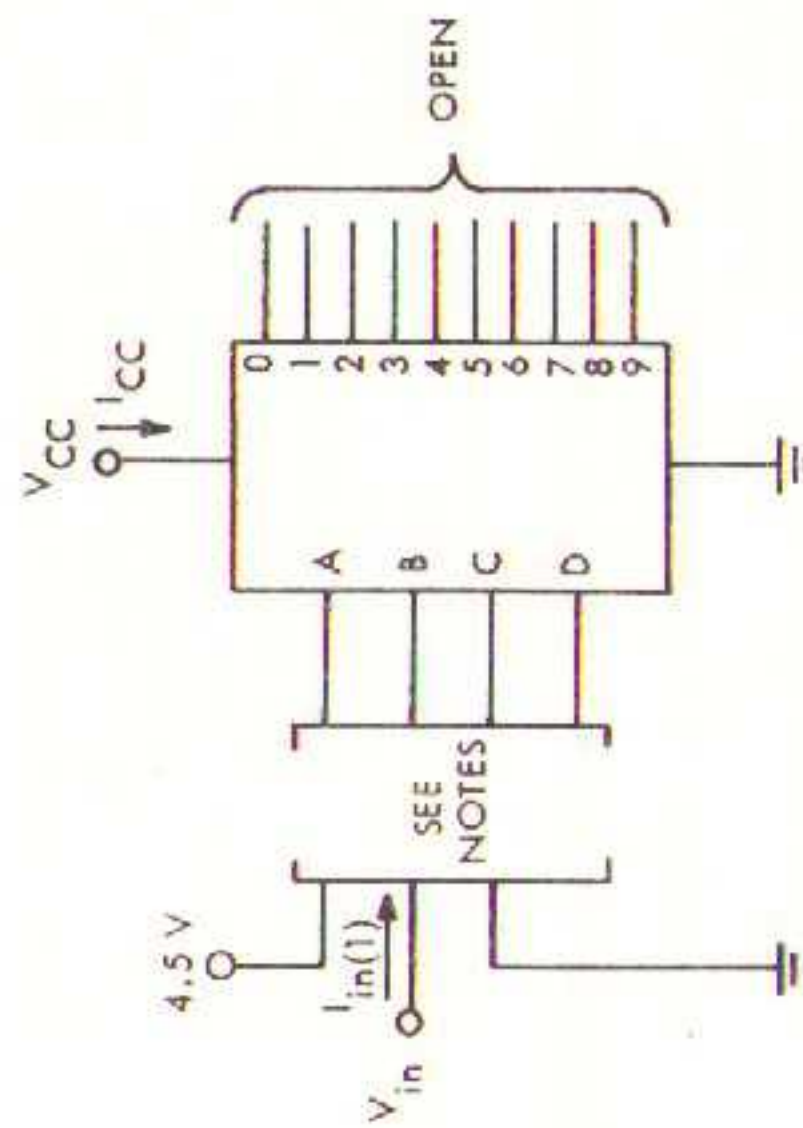


FIGURE 3

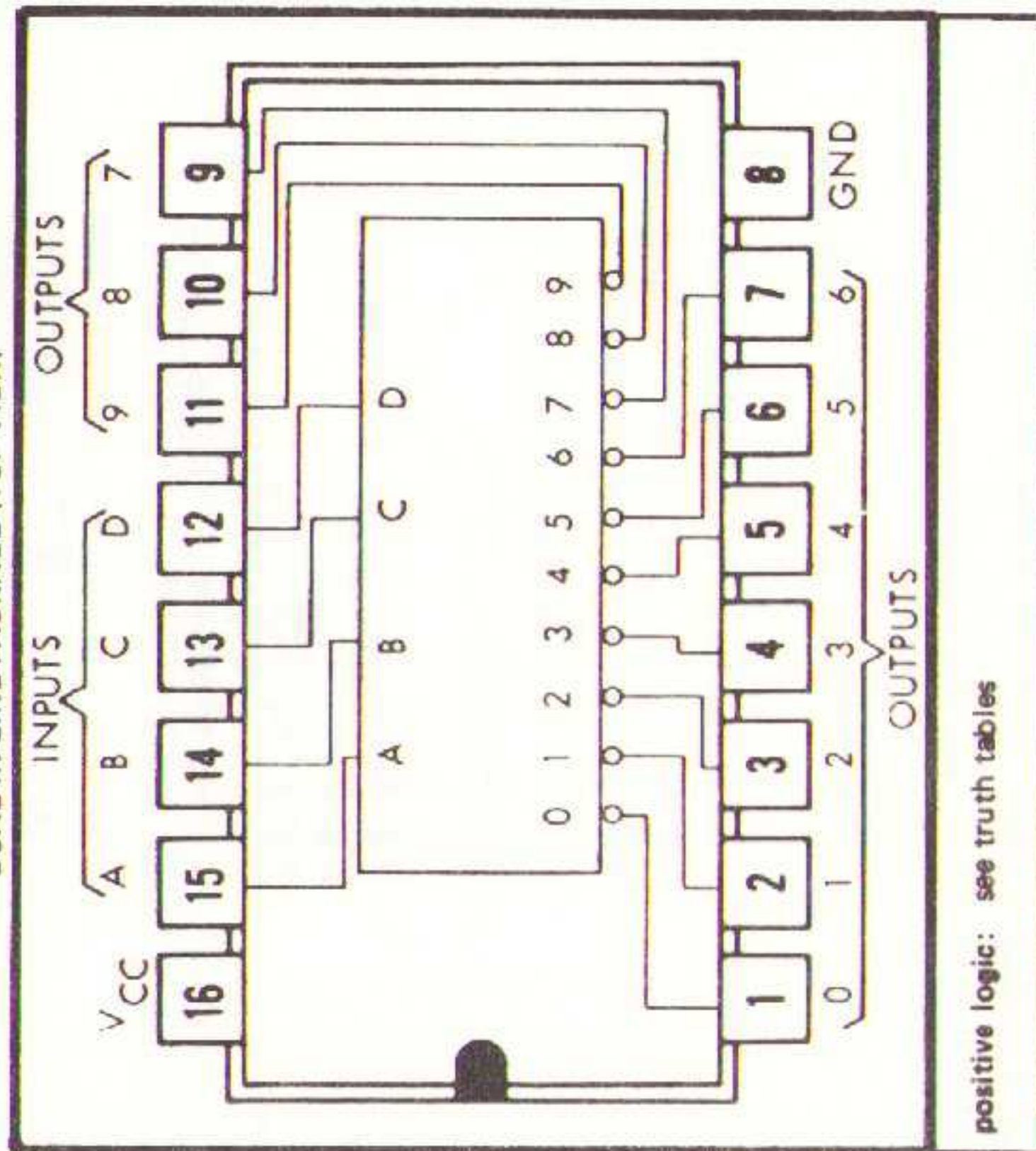
† Arrows indicate actual direction of current flow.

- BCD-to-Decimal
- Excess 3-to-Decimal
- Excess 3 Gray-to-Decimal
- Also for applications as
 - 4-Line to 16-Line Decoders
 - 3-Line to 8-Line Decoders
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess 3-to-decimal, and SN5444/SN7444 excess 3 gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.



SN5442/SN7442				SN5443/SN7443				SN5444/SN7444				ALL TYPES									
BCD INPUT				EXCESS 3 INPUT				EXCESS 3 GRAY INPUT				DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1	1	1	1
0	1	0	0	0	1	1	1	1	0	1	0	1	1	1	0	1	1	1	1	1	1
0	1	0	1	0	1	1	1	1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Note 1)	5.5 V
Operating Free-Air Temperature Range: SN5442, SN5443, SN5444 Circuits	-55°C to 125°C
SN7442, SN7443, SN7444 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

recommended operating conditions (over operating temperature range)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in}(1)$ Input voltage required to ensure logical 1 at any input terminal	1 and 2	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Input voltage required to ensure logical 0 at any input terminal	1 and 2	$V_{CC} = \text{MIN}$		0.8		V
$V_{out}(1)$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$, $V_{in}(1) = 2 \text{ V}$, $V_{in}(0) = 0.8 \text{ V}$, $I_{load} = -400 \mu\text{A}$	2.4			V
$V_{out}(0)$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$, $V_{in}(1) = 2 \text{ V}$, $V_{in}(0) = 0.8 \text{ V}$, $I_{sink} = 16 \text{ mA}$		0.4		V
$I_{in}(1)$ Logical 1 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$		40		μA
$I_{in}(0)$ Logical 0 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$		1		mA
I_{OS} Short-circuit output current§	5	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$		-20		mA
I_{CC} Supply current	4	$V_{CC} = \text{MAX}$, SN5442, SN5443, SN7442, SN7443, SN7444		28		mA

Supply Voltage V_{CC} (See Note 1): SN5442, SN5443, SN5444 Circuits

SN7442, SN7443, SN7444 Circuits

Normalized Fan-Out from each Output (N)

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in}(1)$ Input voltage required to ensure logical 1 at any input terminal	1 and 2	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Input voltage required to ensure logical 0 at any input terminal	1 and 2	$V_{CC} = \text{MIN}$		0.8		V
$V_{out}(1)$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$, $V_{in}(1) = 2 \text{ V}$, $V_{in}(0) = 0.8 \text{ V}$, $I_{load} = -400 \mu\text{A}$	2.4			V
$V_{out}(0)$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$, $V_{in}(1) = 2 \text{ V}$, $V_{in}(0) = 0.8 \text{ V}$, $I_{sink} = 16 \text{ mA}$		0.4		V
$I_{in}(1)$ Logical 1 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$		40		μA
$I_{in}(0)$ Logical 0 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$		1		mA
I_{OS} Short-circuit output current§	5	$V_{CC} = \text{MAX}$, SN5442, SN5443, SN7442, SN7443, SN7444		-20		mA
I_{CC} Supply current	4	$V_{CC} = \text{MAX}$, SN5442, SN5443, SN7442, SN7443, SN7444		28		mA

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level through two logic levels	6	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	10	22	30	ns
t_{pd0} Propagation delay time to logical 0 level through three logic levels	6	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		23	35	ns
t_{pd1} Propagation delay time to logical 1 level through two logic levels	6	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	10	17	25	ns
t_{pd1} Propagation delay time to logical 1 level through three logic levels	6	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		26	35	ns

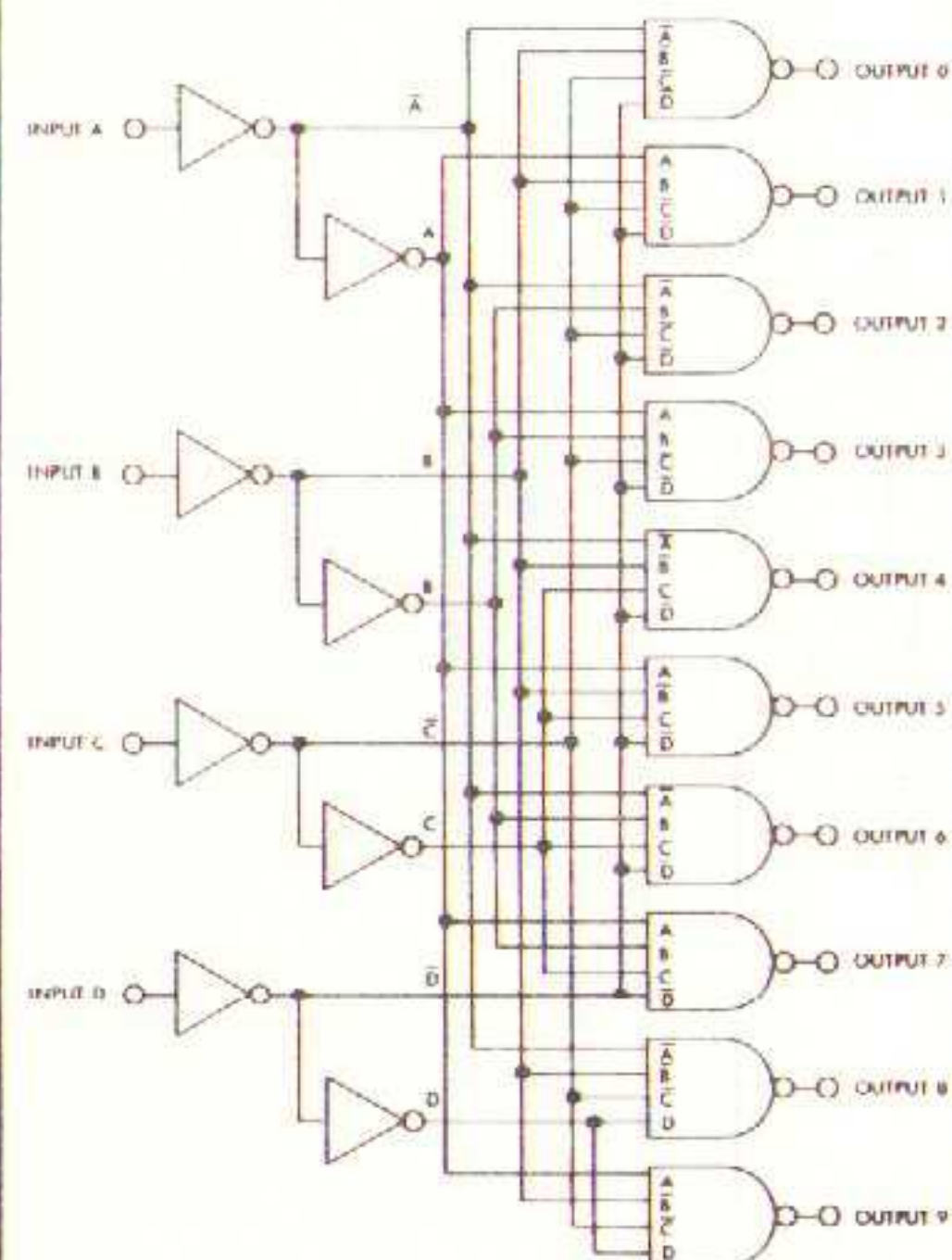
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

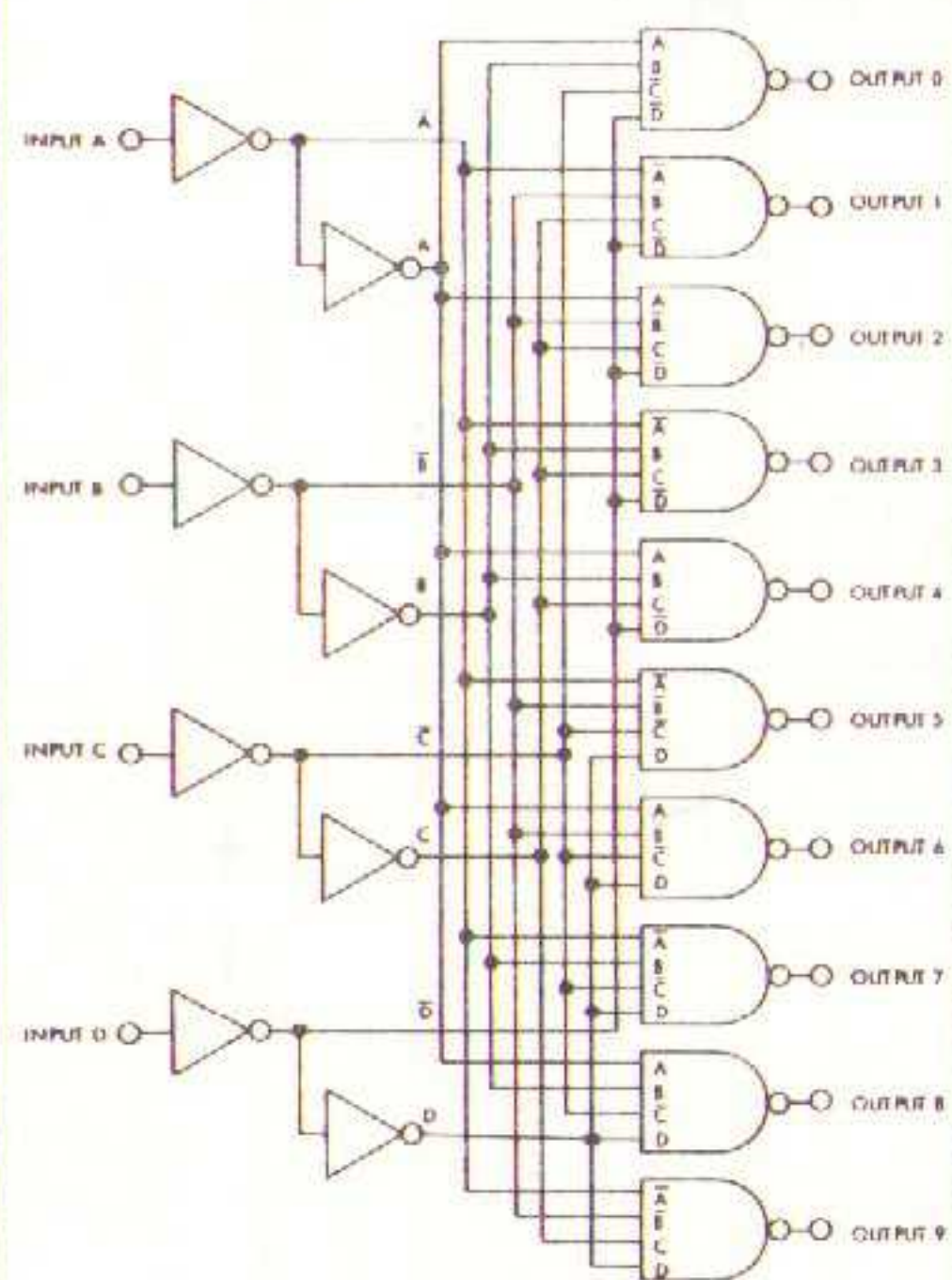
§ Not more than one output should be shorted at a time.

PARAMETER MEASUREMENT INFORMATION

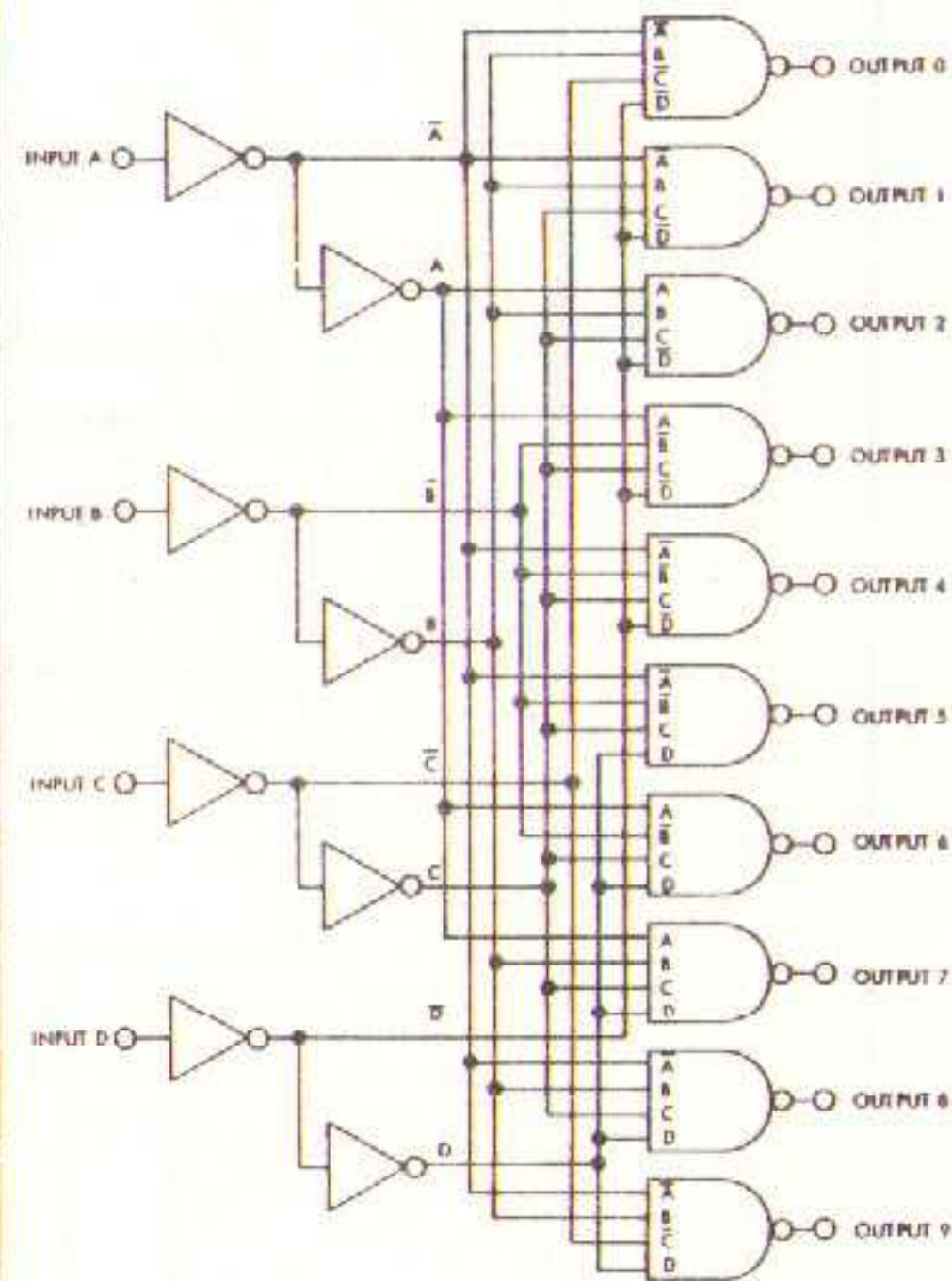
d-c test circuits†



SN5442/SN7442 BCD-TO-DECIMAL



SN5443/SN7443 EXCESS-3-TO-DECIMAL



SN5444/SN7444 EXCESS-3-GRAY-TO-DECIMAL

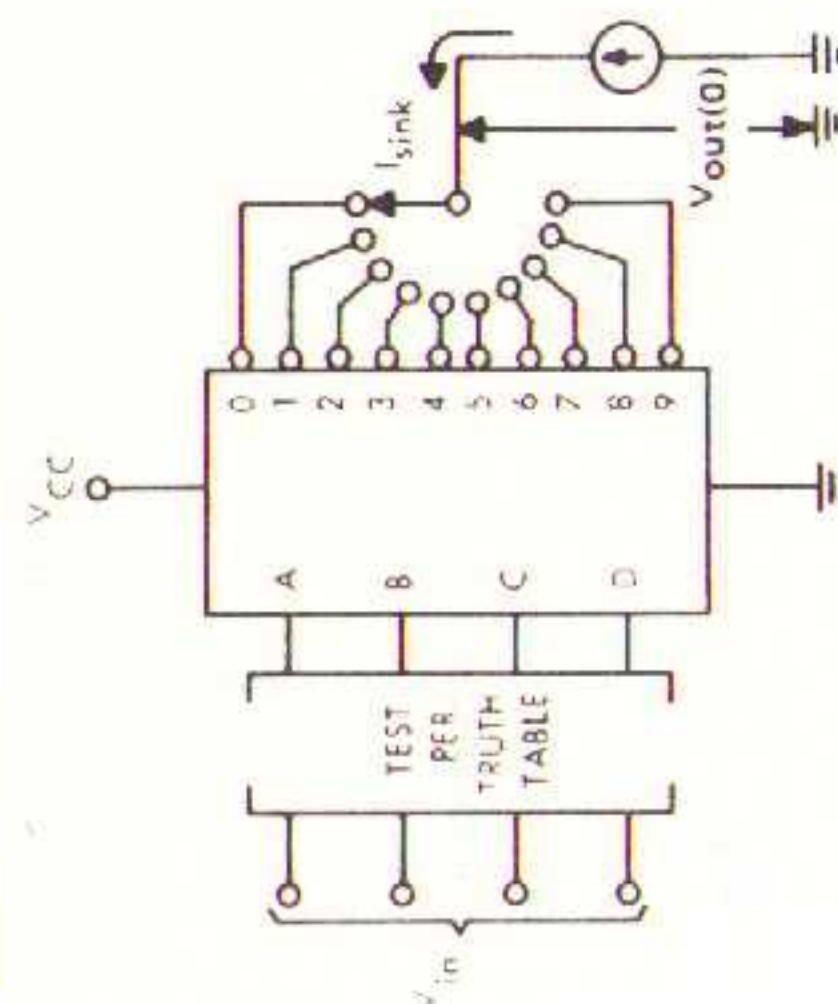


FIGURE 1
1. Each input is tested separately.

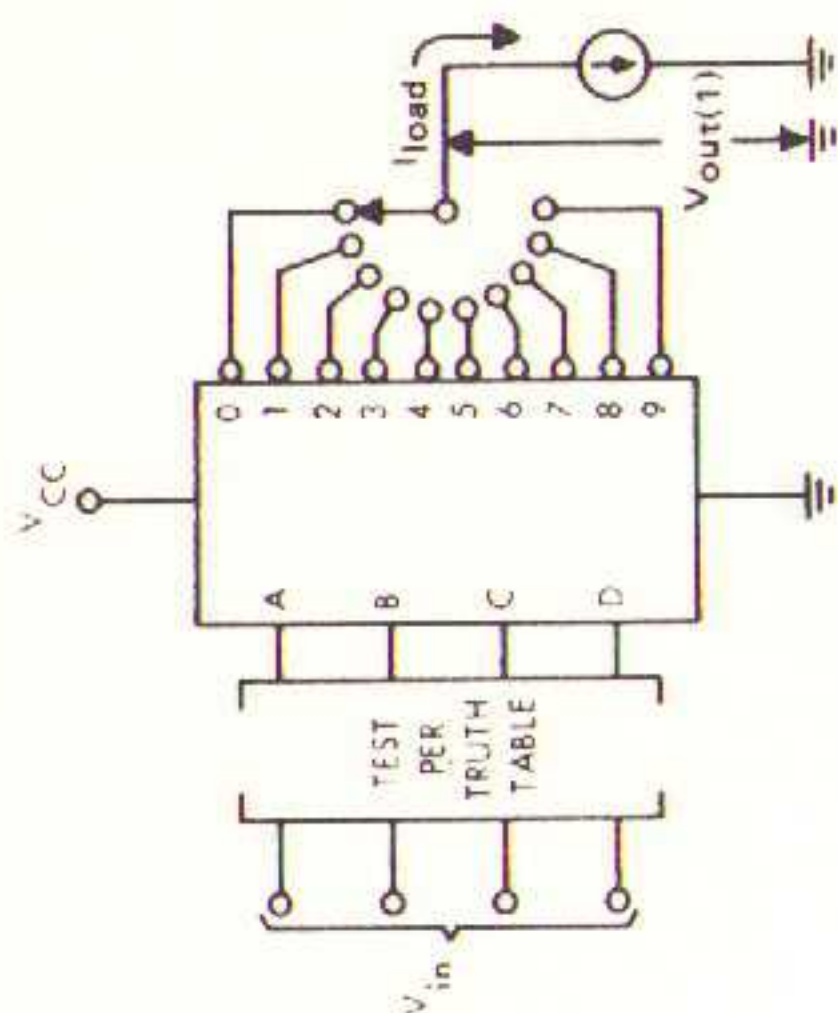


FIGURE 2
1. Each output is tested separately.

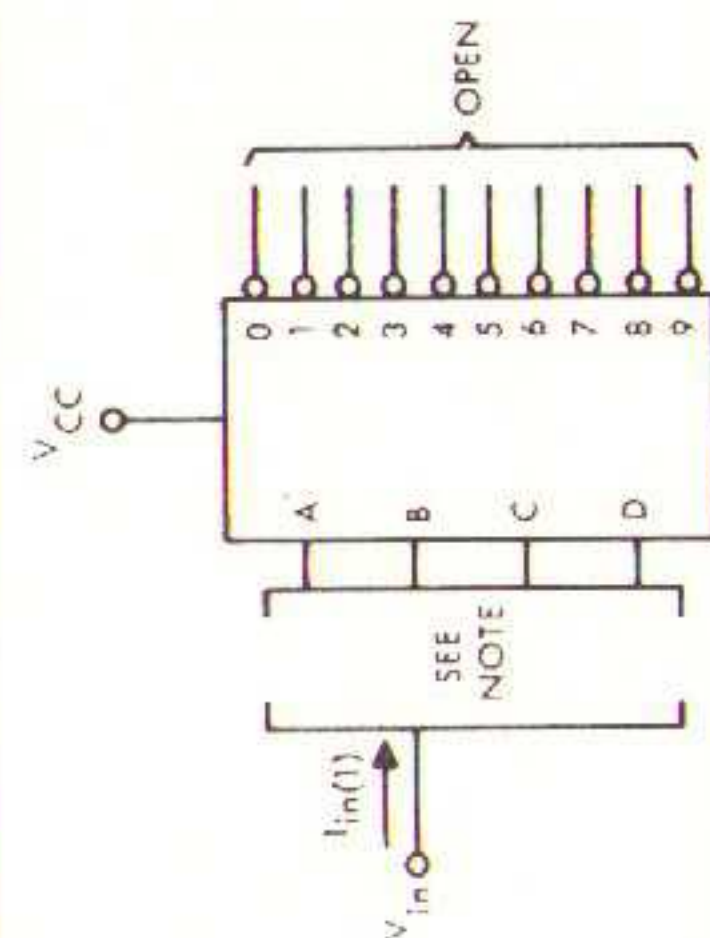


FIGURE 3
1. Each output is tested separately.

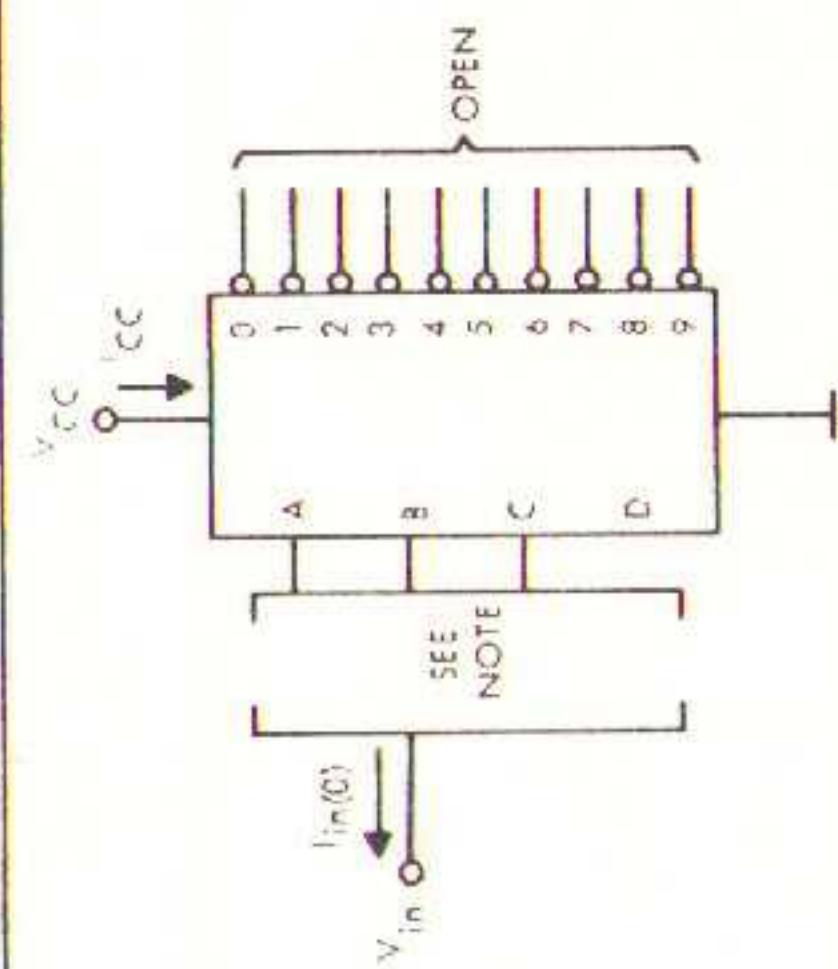


FIGURE 4
1. When testing $I_{in}(0)$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

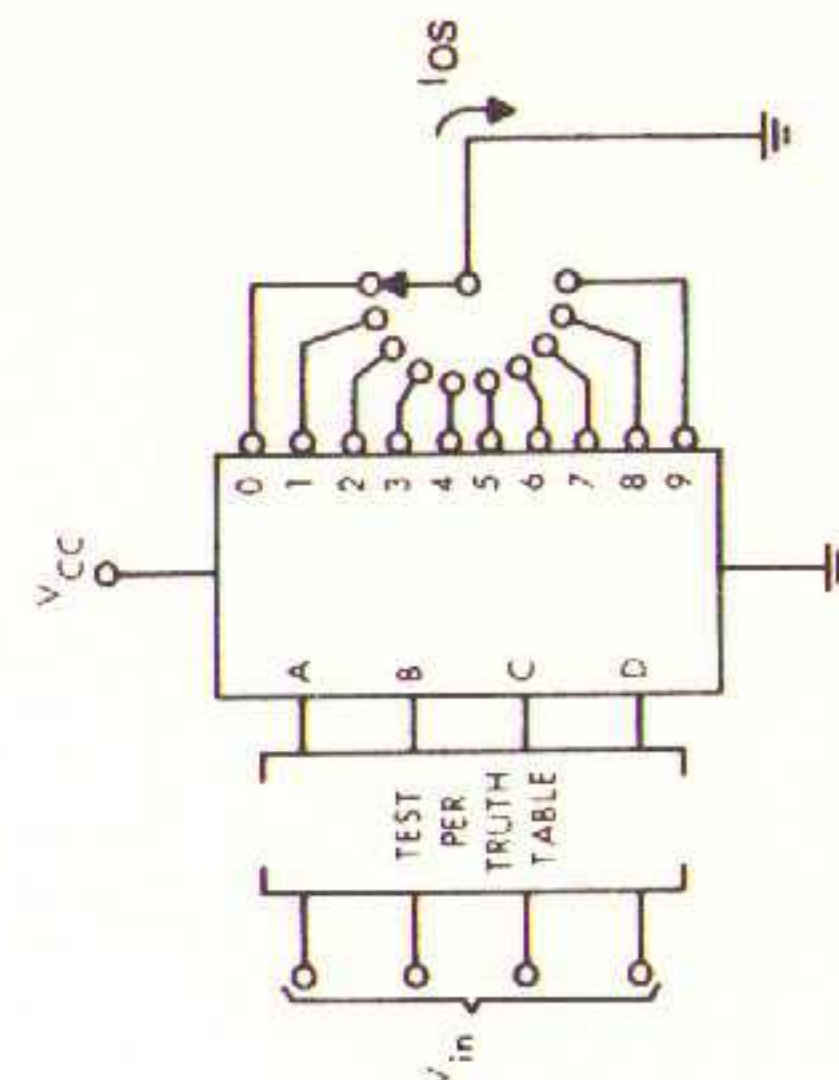


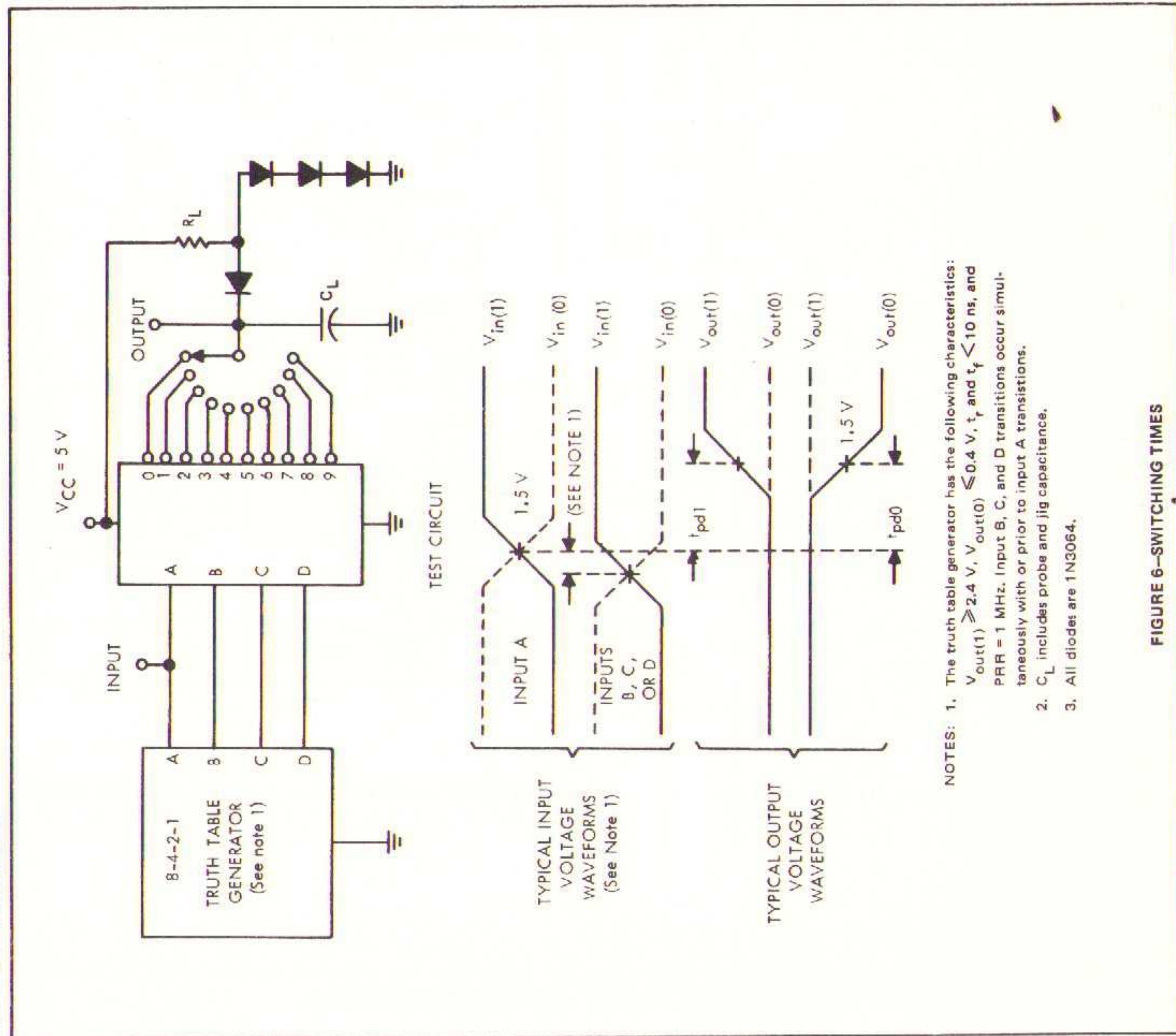
FIGURE 5
1. Each output is tested separately.

†Arrows indicate actual direction of current flow

functional block diagrams

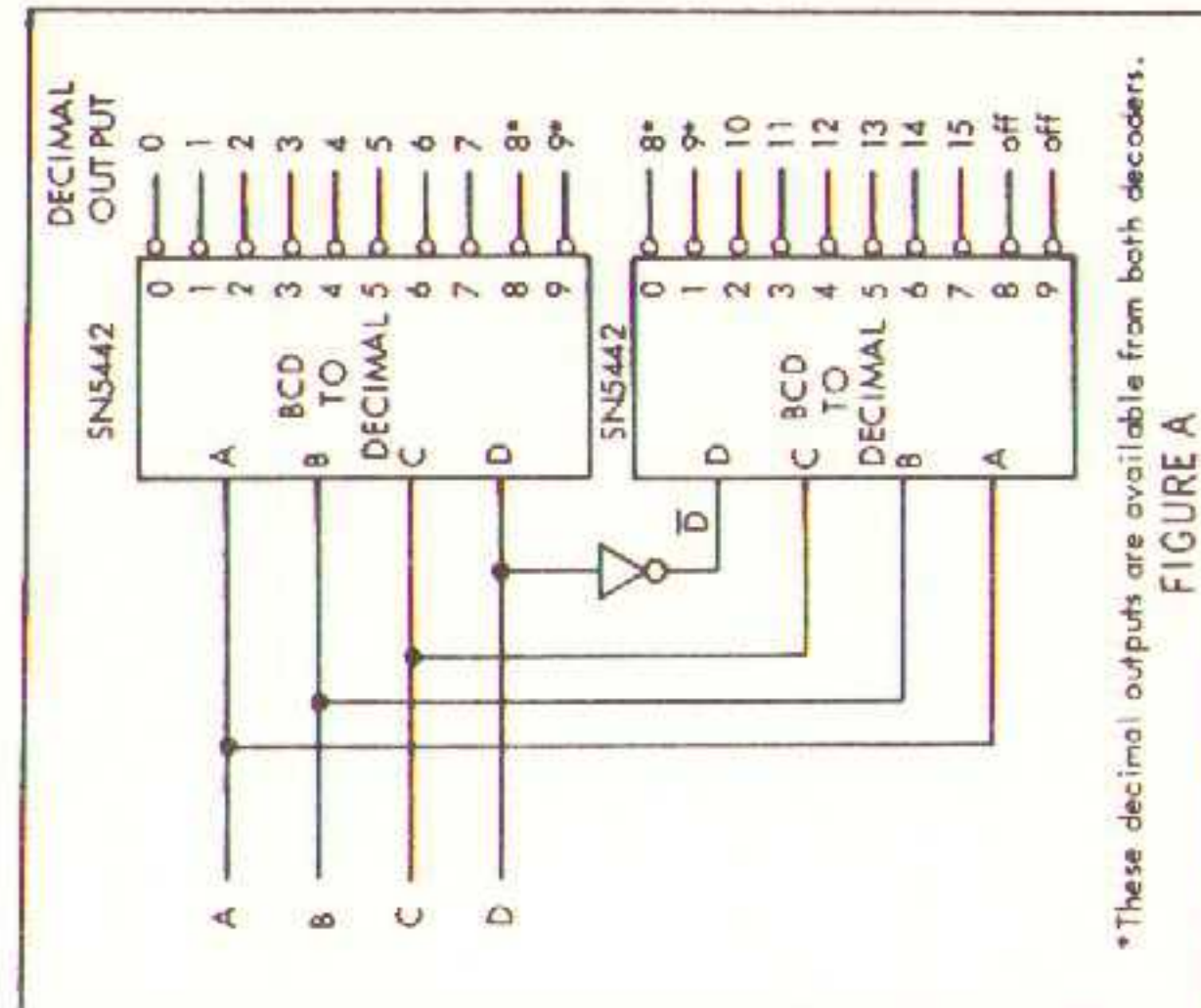
PARAMETER MEASUREMENT INFORMATION

switching characteristics



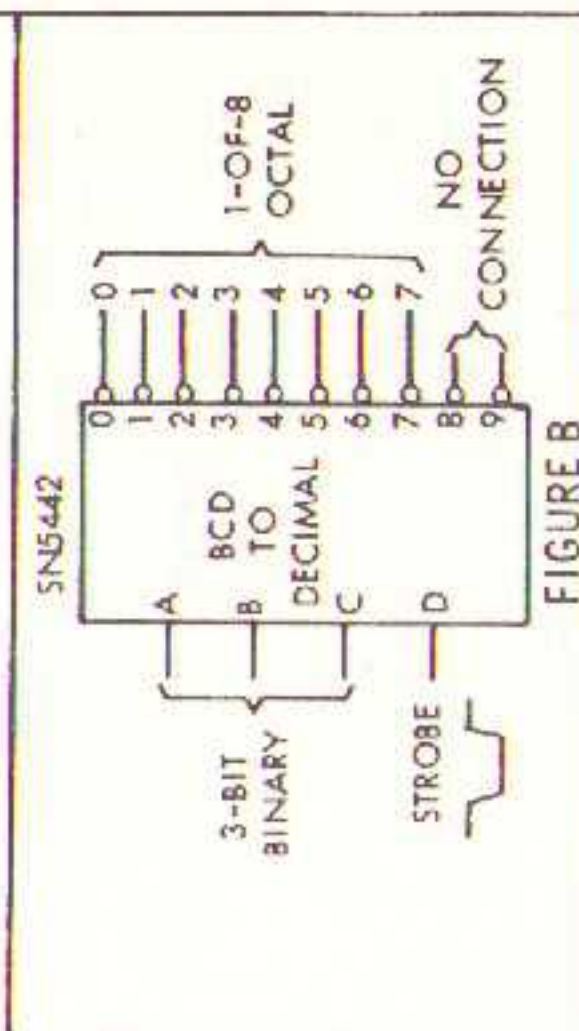
decoding binary-to-decimal with SN5442/SN7442.

Figure A demonstrates a method for utilizing two SN5442/SN7442 decoders to perform 4-wire to 16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, and D is applied to one decoder, and $\bar{D}$ is applied to the other as shown in figure A. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.

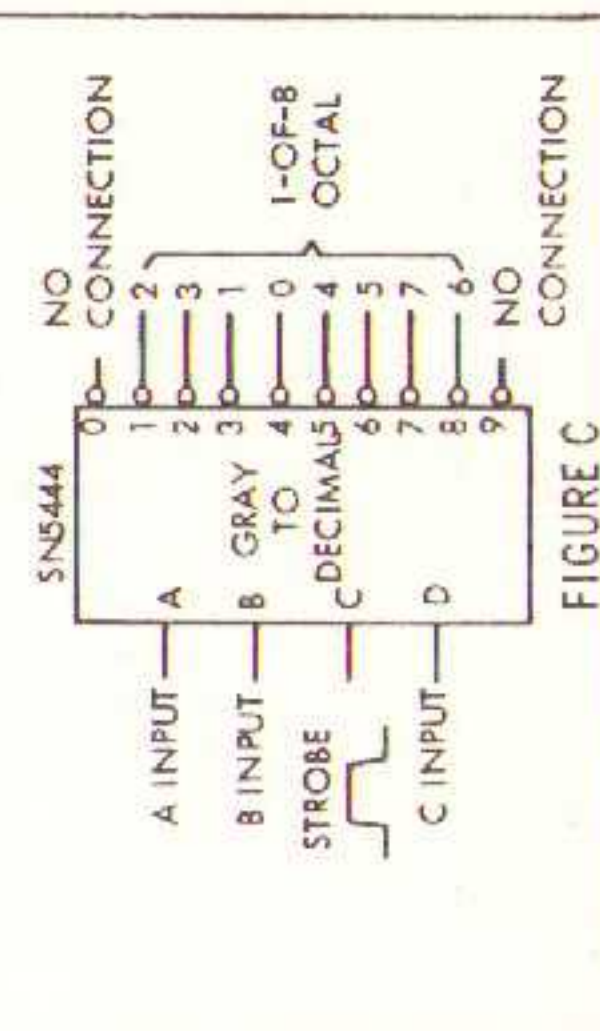


decoding 3-wire binary-to-octal

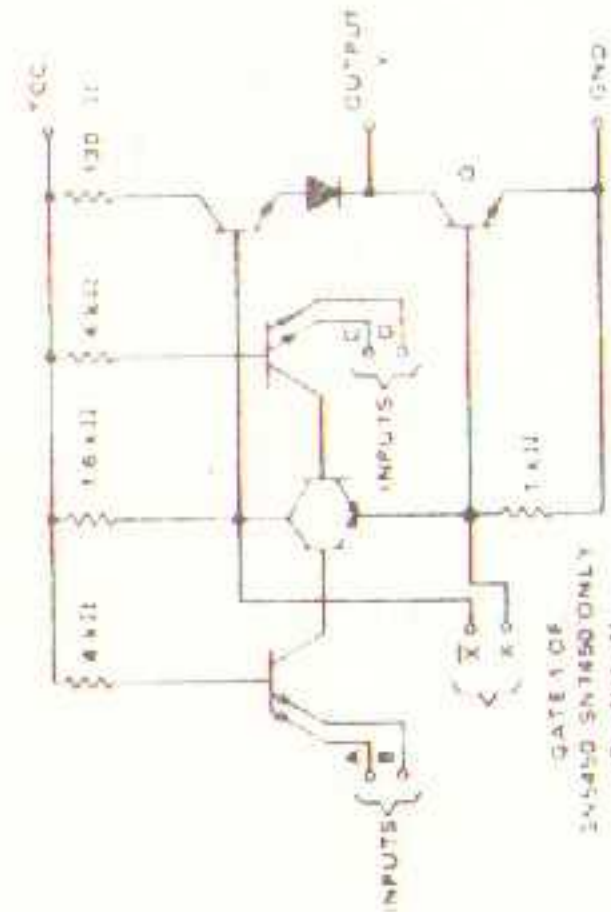
This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5442/SN7442. See figure B. The binary code ABC is applied to the ABC inputs and the D input is used as a strobe. When the strobe is taken to a logical 0 the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.



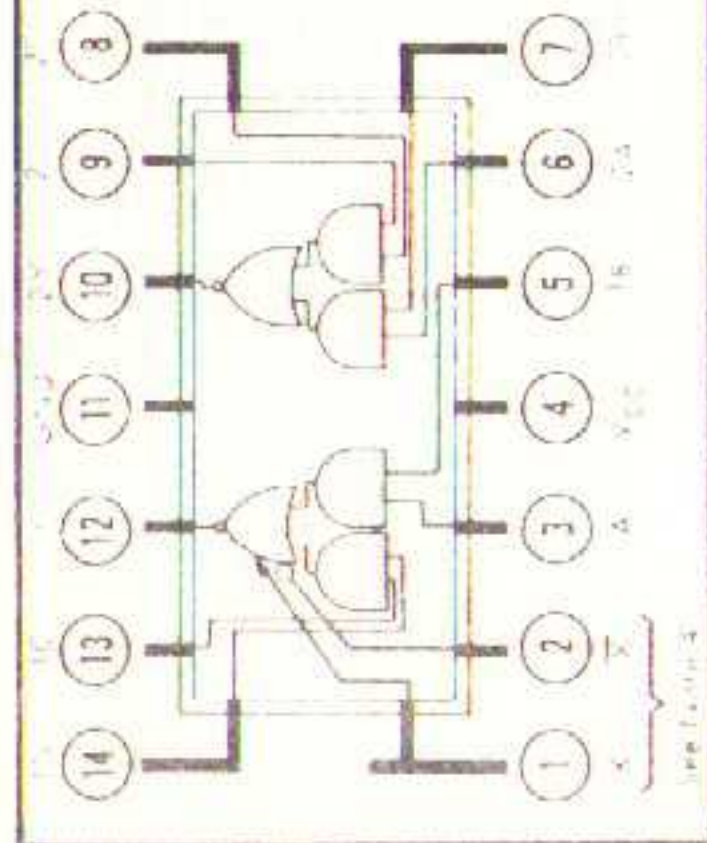
This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5444/SN7444. See figure C. The binary code ABC is applied to the A, B, and C inputs respectively and the D input is used as a strobe. When the strobe is taken to a logical 1 the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.



schematic (each gate)

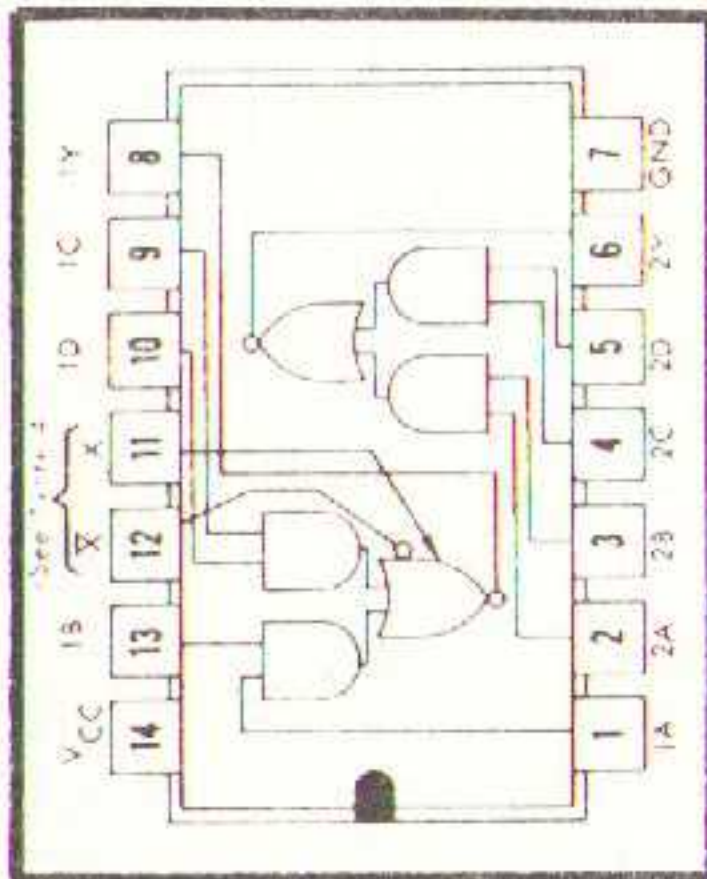


S FLAT PACKAGE (TOP VIEW)



positive logic: Y = (AB) + (CD) + (X)
X = Output of SN5450/SN7450

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



electrical characteristics (SN5450 circuits) using expander inputs, VCC = 4.5 V, TA = -55°C

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IX	28	V1 = 0.4 V, Isink = 16 mA			2.9	mA
VBE(Q) of output transistor (Q)	29	Isink = 16 mA, I1 = 0.41 mA, R1 = 0		1		V
Vout(1)	30	load = -400 μA, I1 = 0.15 mA, I2 = -0.15 mA	2.4	3.3		V
Vout(0)	29	Isink = 16 mA, I1 = 0.3 mA, R1 = 138 Ω	0.22	0.4		V

electrical characteristics (SN7450 circuits) using expander inputs, VCC = 4.75 V, TA = 0°C

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IX	28	V1 = 0.4 V, Isink = 16 mA			3.1	mA
VBE(Q) of output transistor (Q)	29	Isink = 16 mA, I1 = 0.62 mA, R1 = 0		1		V
Vout(1)	30	load = -400 μA, I1 = 270 μA, I2 = -270 μA	2.4	3.3		V
Vout(0)	29	Isink = 16 mA, I1 = 0.43 mA, R1 = 130 Ω	0.22	0.4		V

switching characteristics, VCC = 5 V, TA = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t _{pd0}	65	CL = 15 pF, RL = 400 Ω		8	15	ns
t _{pd1}	65	CL = 15 pF, RL = 400 Ω		13	22	ns

† Expander pins X and X̄ are open.
‡ All typical values are at VCC = 5 V, TA = 25°C.

recommended operating conditions

Supply Voltage VCC	SN5450, SN5451 Circuits	4.5	5	5.5	V
Normalized Fan-Out From Each Output, N	SN7450, SN7451 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, TA	SN5450, SN5451 Circuits	-55	25	125	°C
	SN7450, SN7451 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Vin(1) at both input terminals of either AND section to ensure logical 0 at output	21	VCC = MIN	2			V
Vin(0) at one input terminal of each AND section to ensure logical 1 at output	22	VCC = MIN		0.8		V
Vout(1) Logical 1 output voltage	22	VCC = MIN, Vin = 0.8 V, Iload = -400 μA	2.4	3.3		V
Vout(0) Logical 0 output voltage	21	VCC = MIN, Vin = 2 V, Isink = 16 mA		0.22	0.4	V
Iin(0) Logical 0 level input current (each input)	23	VCC = MAX, Vin = 0.4 V		-1.6		mA
Iin(1) Logical 1 level input current (each input)	24	VCC = MAX, Vin = 2.4 V		40		μA
Ios	25	VCC = MAX, Vin = 5.5 V		1		mA
Icc(0) Logical 0 level supply current	26	VCC = MAX, Vin = 5 V		-20		mA
Icc(1) Logical 1 level supply current	27	VCC = MAX, Vin = 0		-18		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and X̄ are open.
‡ All typical values are at VCC = 5 V, TA = 25°C.
§ Not more than one output should be shorted at a time

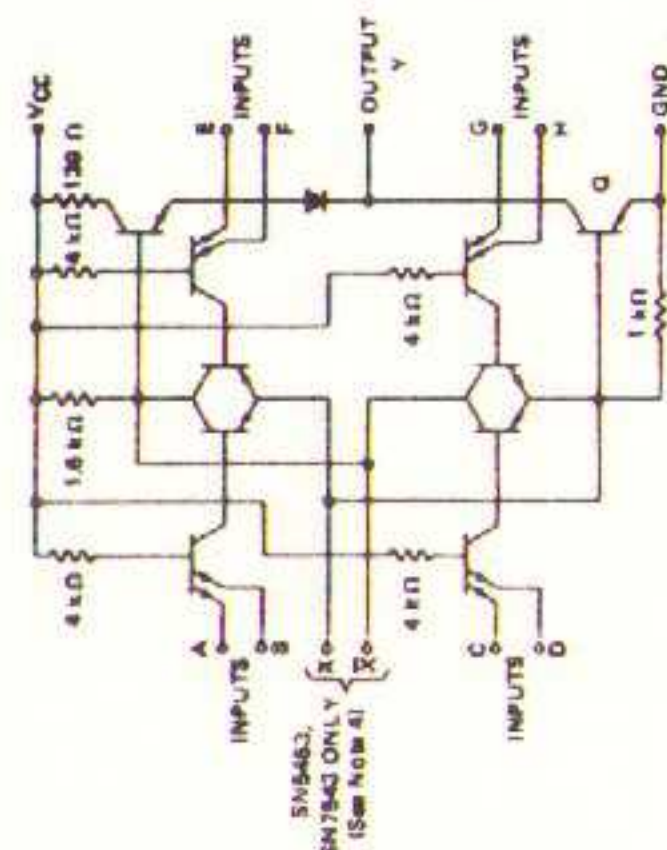
Ontkennen heeft geen zin
..... TTL komt er steeds meer in.
..... zie pag. 76

SN7453

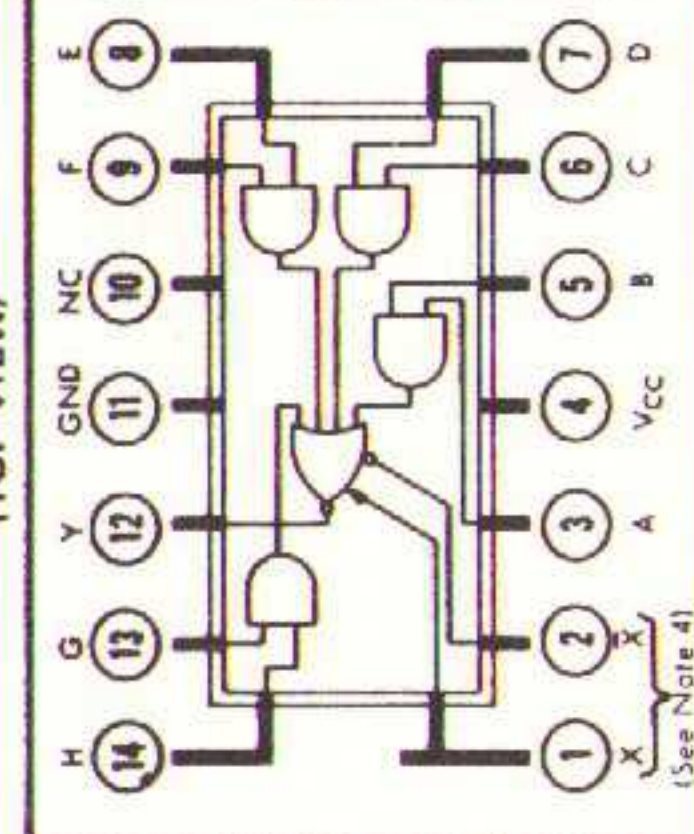
SN7454

EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATES

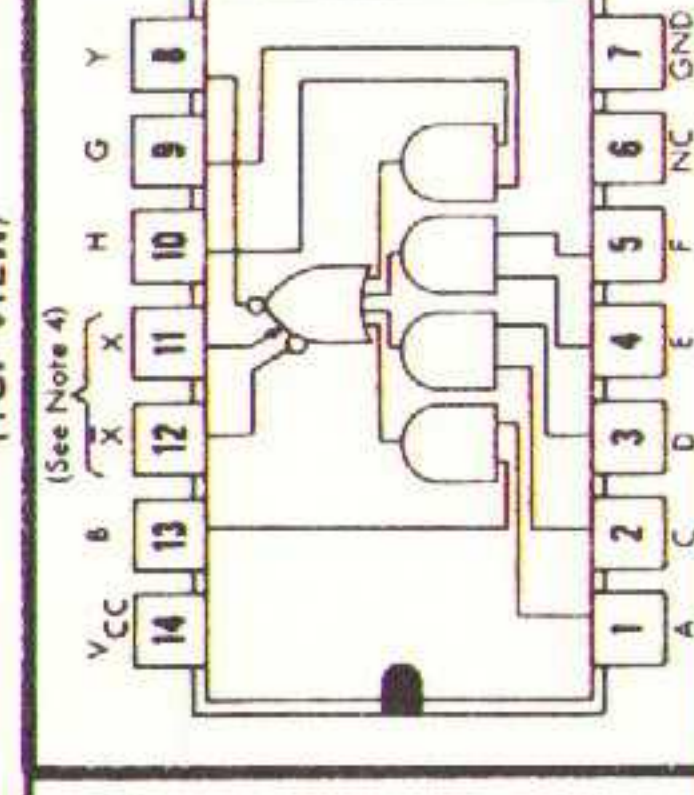
schematic



S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = (AB) + (CD) + (EF) + (GH) + (X)$
X = Output of SN7453/SN7454

- NOTES: 1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and Y pins open.
4. Make no external connection to X and Y pins of the SN7453 and SN7454.
5. A total of four expander gates can be connected to the expander inputs.
6. NC—No Internal Connection

recommended operating conditions

Supply Voltage V_{CC} :	SN7453, SN7454 Circuits	MIN	NOM	MAX	UNIT
	SN7453, SN7454 Circuits	4.5	5	5.5	V
Normalized Fan-Out From Output, N:	SN7453, SN7454 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A :	SN7453, SN7454 Circuits	-55	25	125	$^{\circ}\text{C}$
	SN7453, SN7454 Circuits	0	25	70	$^{\circ}\text{C}$

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	21	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	22	$V_{CC} = \text{MIN}$			0.8	V
$V_{out}(1)$ Logical 1 output voltage	22	$V_{CC} = \text{MIN}$, $V_{in} = 0.8 \text{ V}$, $I_{load} = -400 \mu\text{A}$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	21	$V_{CC} = \text{MIN}$, $V_{in} = 2 \text{ V}$, $I_{sink} = 16 \text{ mA}$		0.22	0.4	V
$I_{in}(0)$ Logical 0 level input current (each input)	23	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in}(1)$ Logical 1 level input current (each input)	24	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$			40	μA
I_{OS} Short-circuit output current [§]	25	$V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$	-20		1	mA
$I_{CC}(0)$ Logical 0 level supply current	26	$V_{CC} = 5.5 \text{ V}$	-18		-55	mA
$I_{CC}(1)$ Logical 1 level supply current	27	$V_{CC} = \text{MAX}$, $V_{in} = 0$	5.1	9.5	8	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and Y are open.
[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.
[§] Not more than one output should be shorted at a time.

Het is logisch, dat mensen, die logische schakelingen ontwikkelen, gebruik maken van TTL logische IC's.

electrical characteristics (SN7453 circuits) using expander inputs, $V_{CC} = 4.5 \text{ V}$, $T_A = -55^{\circ}\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
I_X Expander current	28	$V_1 = 0.4 \text{ V}$, $I_{sink} = 16 \text{ mA}$			2.9	mA
$V_{BE}(Q)$ Base-emitter voltage of output transistor (Q)	29	$I_{sink} = 16 \text{ mA}$, $I_1 = 0.41 \text{ mA}$, $R_1 = 0$			1	V
$V_{out}(1)$ Logical 1 output voltage	30	$I_{load} = -400 \mu\text{A}$, $I_1 = 0.15 \text{ mA}$, $I_2 = -0.15 \text{ mA}$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	29	$I_{sink} = 16 \text{ mA}$, $I_1 = 0.3 \text{ mA}$, $R_1 = 138 \Omega$		0.22	0.4	V

electrical characteristics (SN7473 circuits) using expander inputs, $V_{CC} = 4.75 \text{ V}$, $T_A = 0^{\circ}\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
I_X Expander current	28	$V_1 = 0.4 \text{ V}$, $I_{sink} = 16 \text{ mA}$			3.1	mA
$V_{BE}(Q)$ Base-emitter voltage of output transistor (Q)	29	$I_{sink} = 16 \text{ mA}$, $I_1 = 0.62 \text{ mA}$, $R_1 = 0$			1	V
$V_{out}(1)$ Logical 1 output voltage	30	$I_{load} = -400 \mu\text{A}$, $I_1 = 270 \mu\text{A}$, $I_2 = -270 \mu\text{A}$	2.4	3.3		V
$V_{out}(0)$ Logical 0 output voltage	29	$I_{sink} = 16 \text{ mA}$, $I_1 = 0.43 \text{ mA}$, $R_1 = 130 \Omega$		0.22	0.4	V

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, $N = 10$

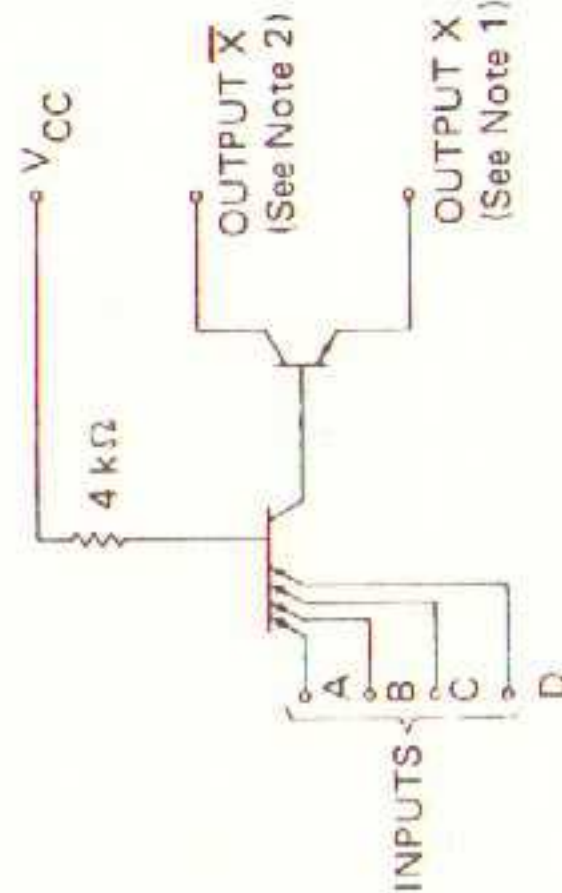
PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		8	15	ns
t_{pd1} Propagation delay time to logical 1 level	65	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		13	22	ns

[†] Expander inputs X and Y are open.
[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

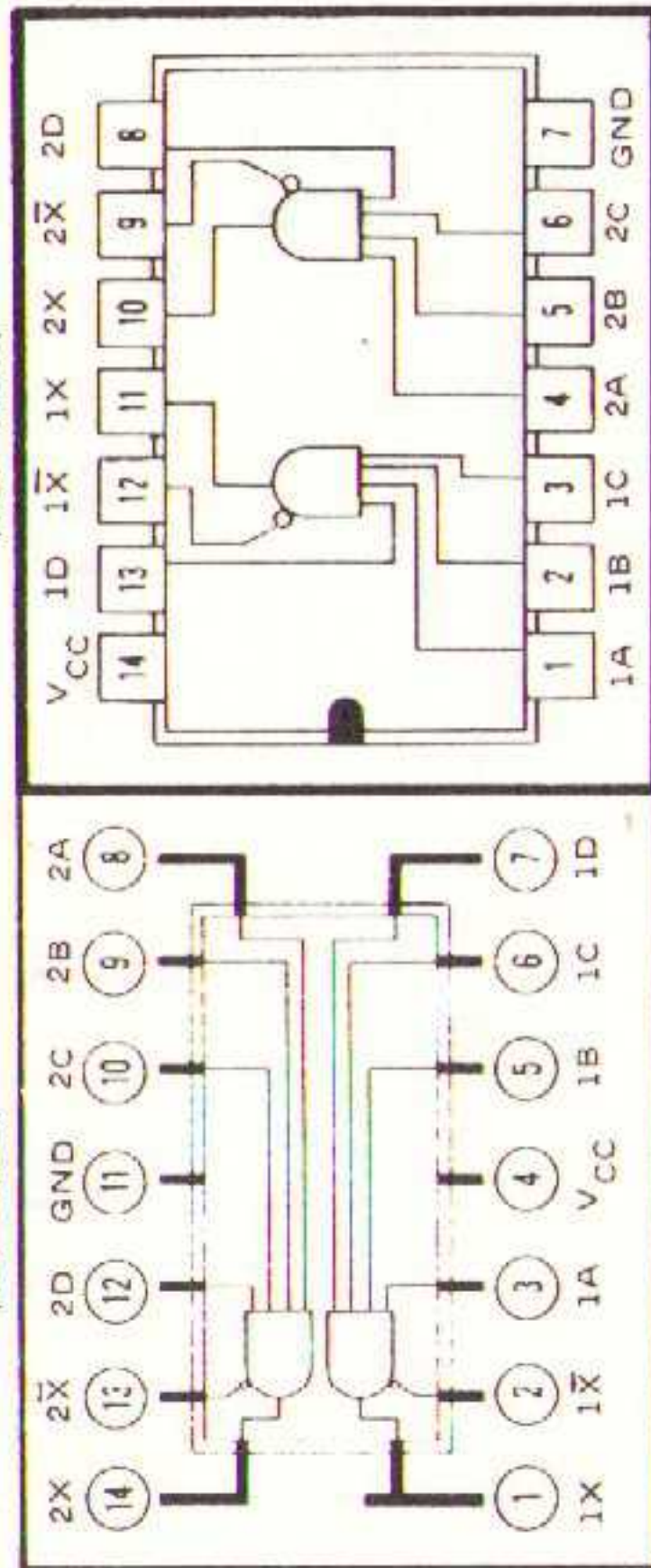
SN7460

DUAL 4-INPUT EXPANDER

schematic (each expander)



S FLAT PACKAGE (TOP VIEW)



positive logic: X=ABCD
when connected to X and X pins of SN7450 or SN7453 circuit.

- NOTES: 1. Connect to X input of SN7450 or SN7453 circuit.
2. Connect to X input of SN7450 or SN7453 circuit.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN7450 or one SN7453 Circuit 4

electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to 70°C)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage required at all input terminals is in the on state	31	$V_{CC} = 4.75\text{ V}$	2			V
$V_{in}(0)$ Logical 0 input voltage required at any input terminal is in the off state	32	$V_{CC} = 4.75\text{ V}$			0.8	V
V_{on} On-state output voltage	31	$V_{CC} = 4.75\text{ V}, V_{in} = 2\text{ V}, V_1 = 1\text{ V}, R = 1.1\text{ k}\Omega, T_A = 0^\circ\text{C}$			0.4	V
I_{off} Off-state output current	32	$V_{CC} = 4.75\text{ V}, V_{in} = 0.8\text{ V}, V_1 = 4.5\text{ V}, R = 1.2\text{ k}\Omega, T_A = 0^\circ\text{C}$			270	μA
I_{on} On-state output current	33	$V_{CC} = 4.75\text{ V}, V_{in} = 2\text{ V}, V_1 = 1\text{ V}$	-0.43			mA
$I_{in}(0)$ Logical 0 level input current (each input)	32	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in}(1)$ Logical 1 level input current (each input)	34	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$			40	μA
$I_{CC}(on)$ On-state supply current	35	$V_{CC} = 5.25\text{ V}, V_{in} = 5\text{ V}, V_1 = 0.85\text{ V}$		1.2	2.5	mA
$I_{CC}(off)$ Off-state supply current	35	$V_{CC} = 5.25\text{ V}, V_{in} = 0, V_1 = 0.85\text{ V}$		2	4	mA

[†] All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level (through SN7450 or SN7453)	66	$C_L = 15\text{ pF}, R_L = 400\ \Omega$		10	20	ns
t_{pd1} Propagation delay time to logical 1 level (through SN7450 or SN7453)	66	$C_L = 15\text{ pF}, R_L = 400\ \Omega$		15	30	ns

SN7470

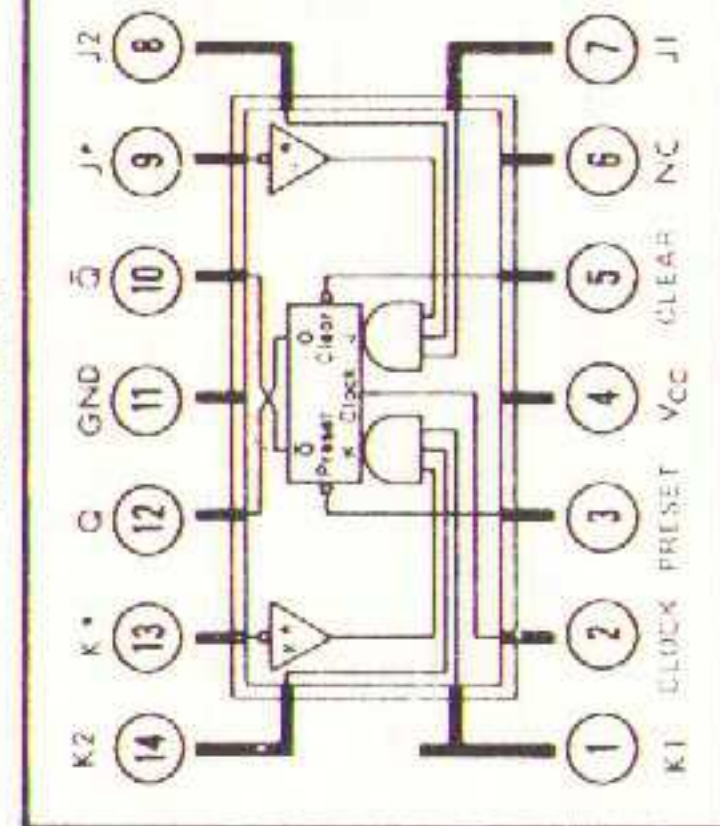
EDGE-TRIGGERED J-K FLIP-FLOPS

logic

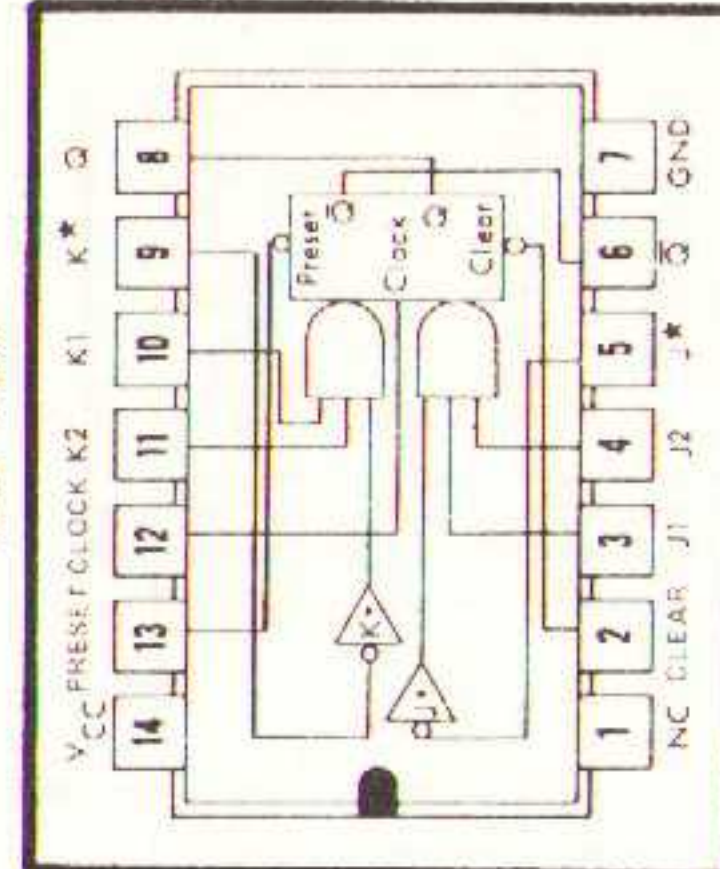
TRUTH TABLE			
J	K	t_n	Q_{n+1}
0	0	0	0
0	1	0	0
1	0	1	1
1	1	1	$\bar{Q}_n$

- NOTES: 1. $J = J_1 + J_2 + J_3$
2. $K = K_1 + K_2 + K_3$
3. t_n = Bit time before clock pulse.
4. $t_n - 1$ = Bit time after clock pulse.
5. If inputs J_3 or K_3 are not used, they must be grounded.
6. NC = No Internal Connection

S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\bar{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium- to high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

Supply Voltage V_{CC} :	SN5470 Circuits	4.5	5	5.5	V
	SN7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A :	SN5470 Circuits	-55	25	125	$^\circ\text{C}$
	SN7470 Circuits	0	25	70	$^\circ\text{C}$
Normalized Fan-Out From Each Output, N			10		
Clock Pulse Transition Time to Logical 1 Level, $t_1(\text{clock})$ (See Figure 68)		5	150		ns
Width of Clock Pulse, $t_p(\text{clock})$ (See Figure 68)		20			ns
Width of Preset Pulse, $t_p(\text{preset})$ (See Figure 67)		25			ns
Width of Clear Pulse, $t_p(\text{clear})$ (See Figure 67)		25			ns

Wees niet van gisteren, gebruik vandaag TTL.

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	36 and 37	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	36 and 37	$V_{CC} = \text{MIN}$		0.8		V
$V_{out(1)}$ Logical 1 output voltage	36	$V_{CC} = \text{MIN}$, $I_{load} = -400 \mu\text{A}$	2.4	3.5		V
$V_{out(0)}$ Logical 0 output voltage	37	$V_{CC} = \text{MIN}$, $I_{sink} = 16 \text{ mA}$	0.22	0.4		V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J*, J1, K2, K*, or clock	38	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$		-1.6		mA
$I_{in(0)}$ Logical 0 level input current at preset or clear	38	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$		-3.2		mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	39	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$		40		μA
$I_{in(1)}$ Logical 1 level input current at preset or clear	39	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$		80		μA
I_{OS} Short-circuit output current§	40	$V_{CC} = \text{MAX}$, $V_{in} = 0$	-20	-57		mA
I_{CC} Supply current	39	$V_{CC} = \text{MAX}$, $V_{in} = 5 \text{ V}$	-18	-57		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

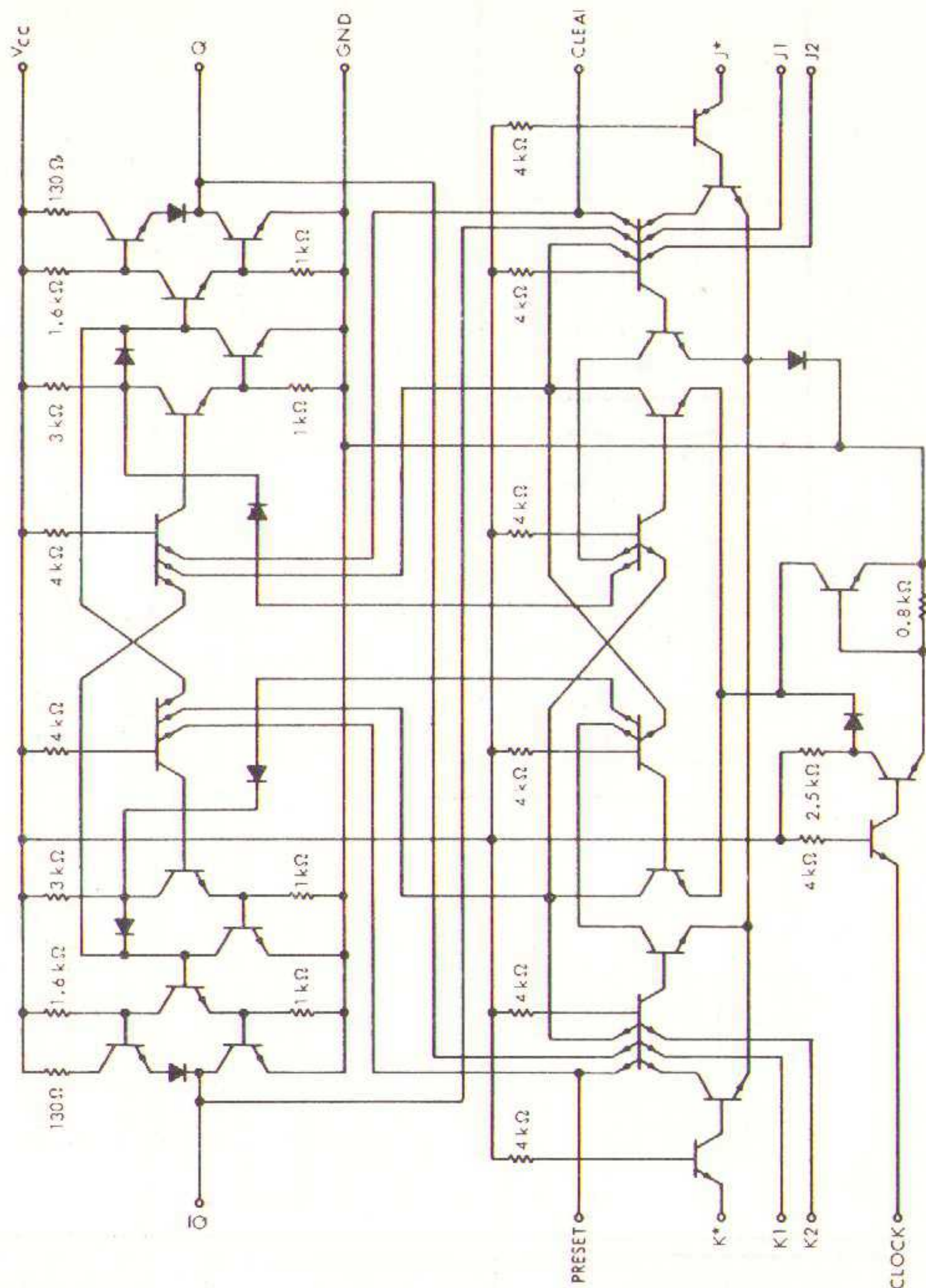
‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock} Maximum clock frequency	68	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	20	35		MHz
t_{setup} Minimum input setup time	68	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	10	20		ns
t_{hold} Minimum input hold time	68	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	0	5		ns
t_{pd1} Propagation delay time to logical 1 level from clear or preset to output	67	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		50		ns
t_{pd0} Propagation delay time to logical 0 level from clear or preset to output	67	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		50		ns
t_{pd1} Propagation delay time to logical 1 level from clock to output	68	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	10	27	50	ns
t_{pd0} Propagation delay time to logical 0 level from clock to output	68	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$	10	18	50	ns

schematic



NOTE: Component values shown are nominal.

logic

TRUTH TABLE			
J	K	t_n	Q_n
0	0	0	0
0	1	0	0
1	0	1	1
1	1	1	$\bar{Q}_n$

- NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC = No Internal Connection.

description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

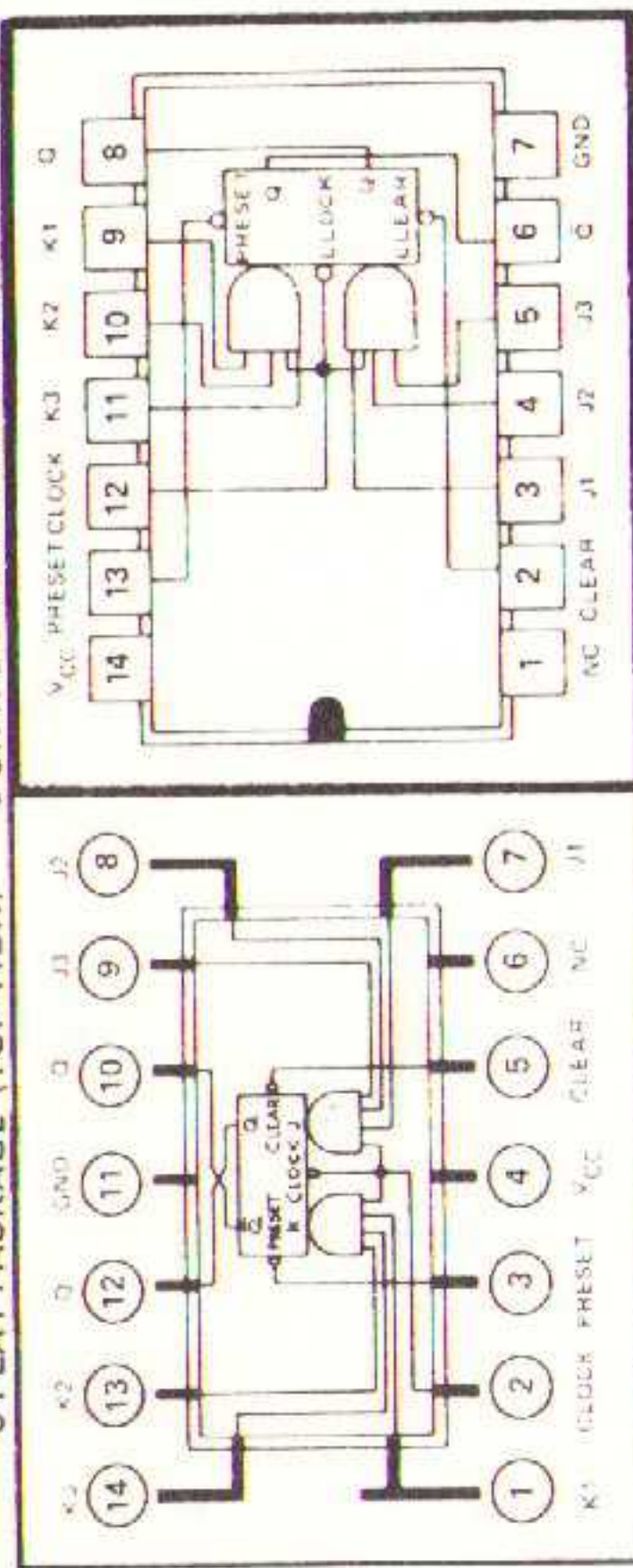
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

recommended operating conditions

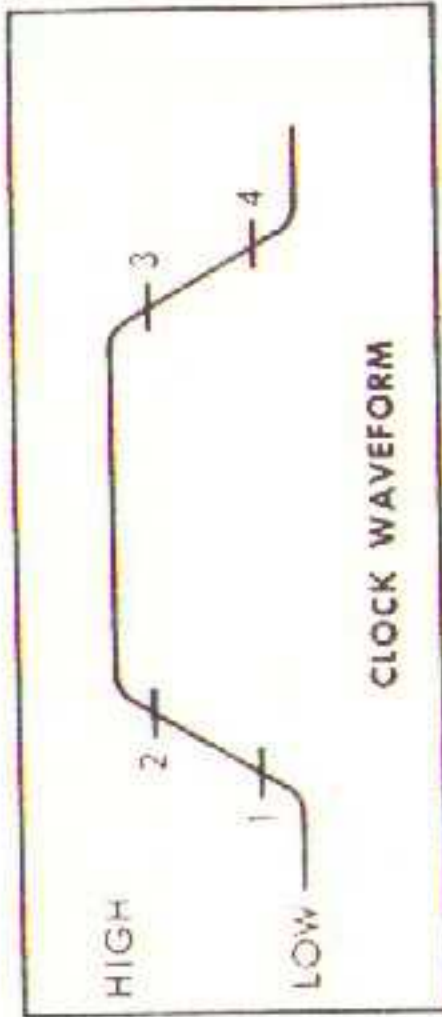
Supply Voltage VCC:	SN5472 Circuits	SN7472 Circuits	
Operating Free-Air Temperature Range, T _A :	SN5472 Circuits	SN7472 Circuits	
Normalized Fan-Out From Each Output, N			
Width of Clock Pulse, t _p (clock)	(See figure 69)		
Width of Preset Pulse, t _p (preset)	(See figure 70)		
Width of Clear Pulse, t _p (clear)	(See figure 70)		
Input Setup Time, t _{setup}	(See figure 69)		
Input Hold Time, t _{hold}			

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
-55	25	125	°C
0	25	70	°C
		10	
20			ns
25			ns
25			ns
$\geq t_{p(\text{clock})}$			
0			

S FLAT PACKAGE (TOP VIEW) J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock



electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{in} (1)	41 and 42	V _{CC} = MIN	2			V
V _{in} (0)	41 and 42	V _{CC} = MIN		0.8		V
V _{out} (1)	41	V _{CC} = MIN, I _{load} = -400 µA	2.4	3.5		V
V _{out} (0)	42	V _{CC} = MIN, I _{sink} = 16 mA		0.22	0.4	V
I _{in} (0)	43	V _{CC} = MAX, V _{in} = 0.4 V			-1.6	mA
I _{in} (0)	43	V _{CC} = MAX, V _{in} = 0.4 V			-3.2	mA
I _{in} (1)	44	V _{CC} = MAX, V _{in} = 2.4 V			40	µA
I _{in} (1)	44	V _{CC} = MAX, V _{in} = 5.5 V			1	mA
I _{in} (1)	44	V _{CC} = MAX, V _{in} = 2.4 V			80	µA
I _{in} (1)	44	V _{CC} = MAX, V _{in} = 5.5 V			1	mA
I _{OS}	45	V _{CC} = MAX, V _{in} = 0	SN5472	-20	-57	mA
I _{CC}	44	V _{CC} = MAX, V _{in} = 5 V	SN7472	-18	-57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§ Not more than one output should be shorted at a time.

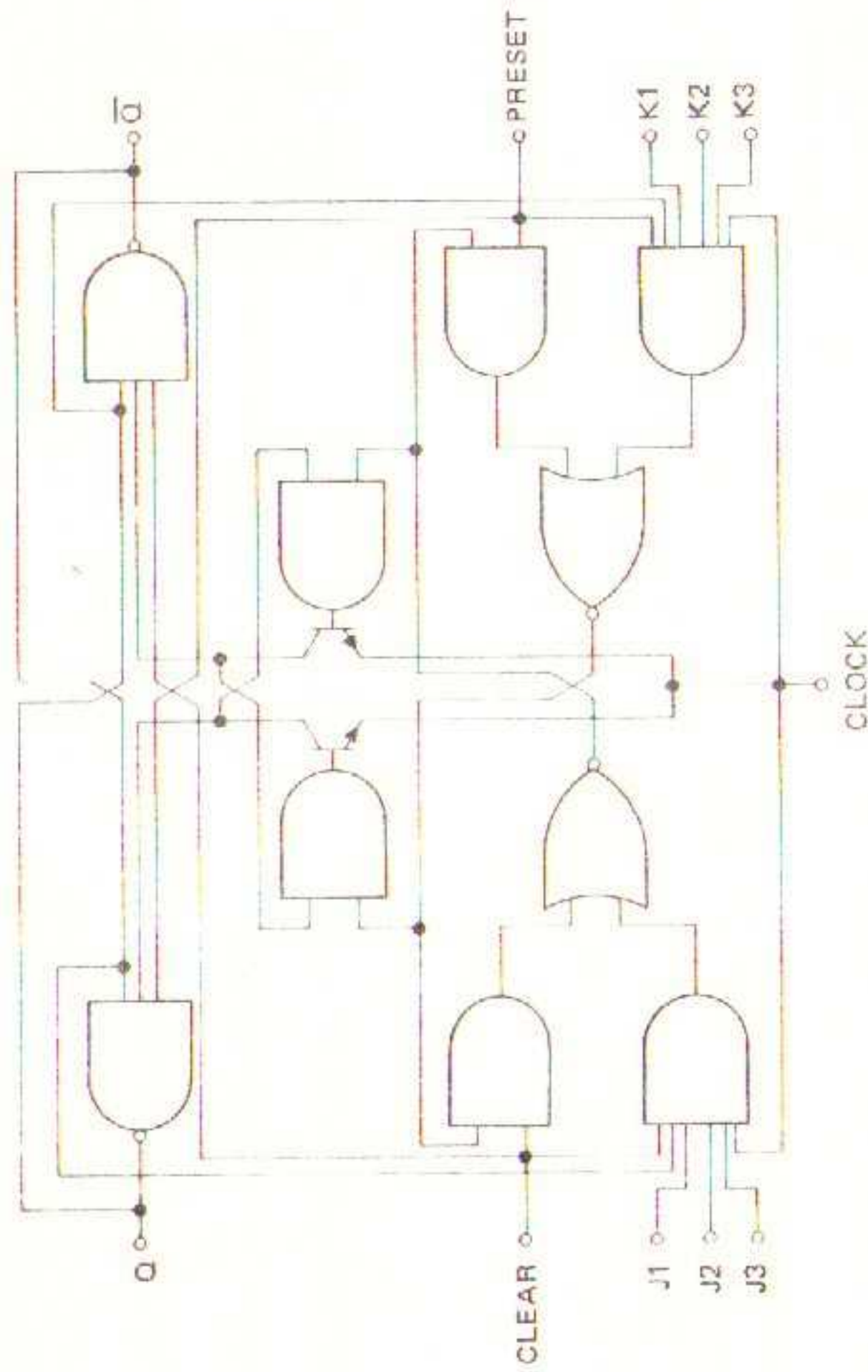
switching characteristics, V_{CC} = 5 V, T_A = 25 °C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{clock}	69	C _L = 15 pF, R _L = 400 Ω	15	20		MHz
t _{pd1}	70	C _L = 15 pF, R _L = 400 Ω		16	25	ns
t _{pd0}	70	C _L = 15 pF, R _L = 400 Ω		25	40	ns
t _{pd1}	69	C _L = 15 pF, R _L = 400 Ω	10	16	25	ns
t _{pd0}	69	C _L = 15 pF, R _L = 400 Ω	10	25	40	ns

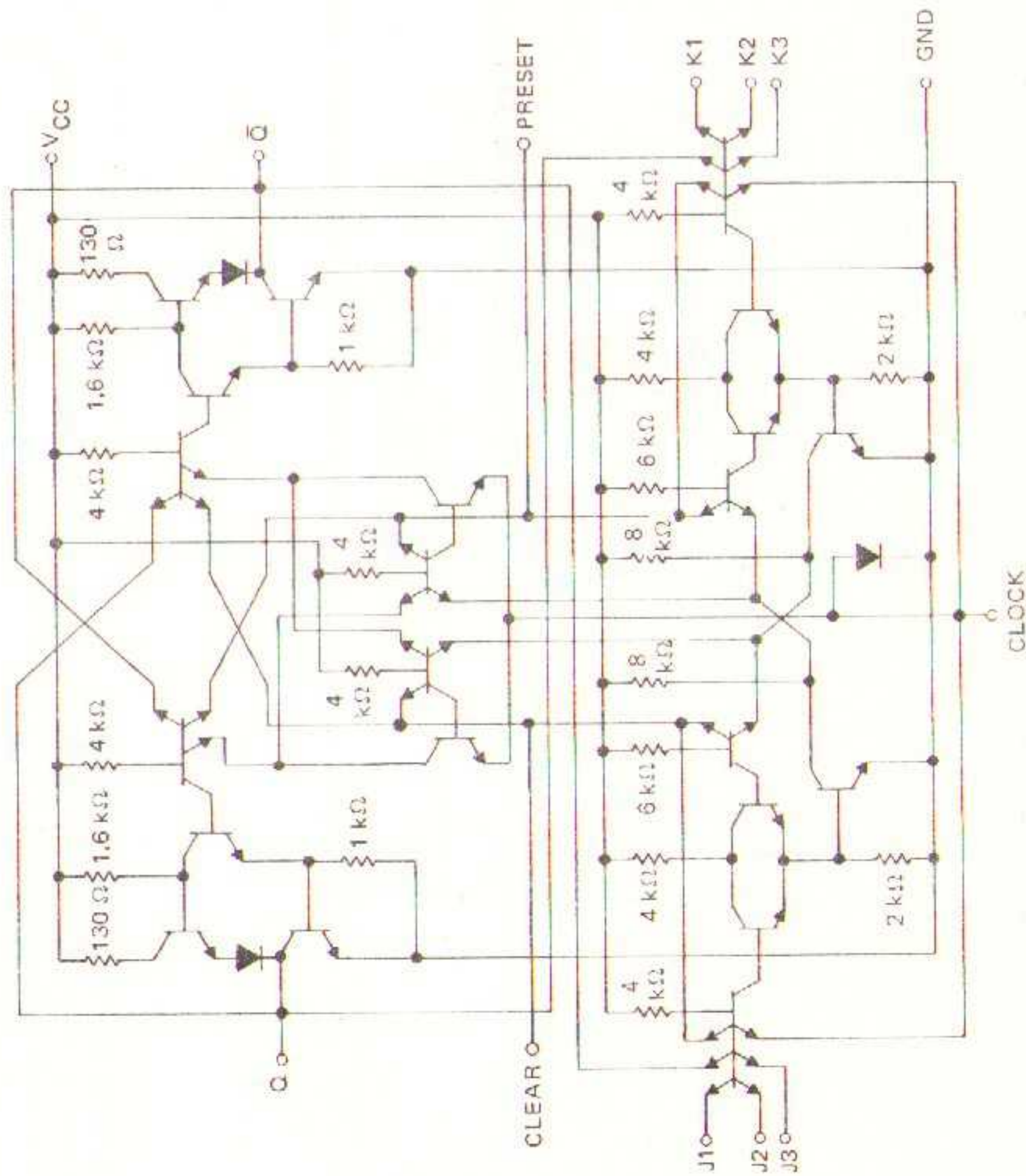
SN7472

J-K MASTER-SLAVE FLIP-FLOPS

functional block diagram



schematic

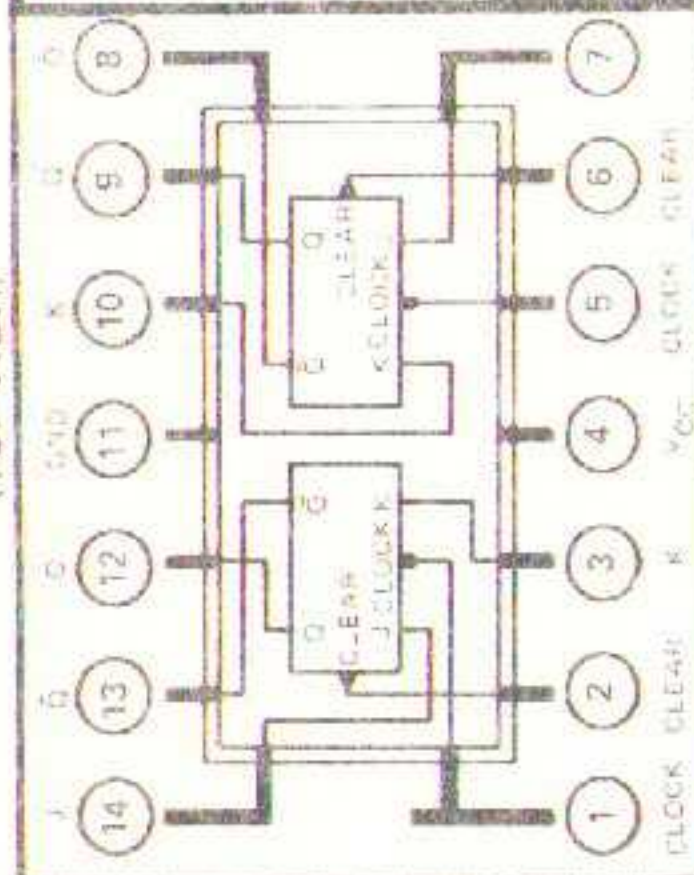


NOTES: Component values shown are nominal.

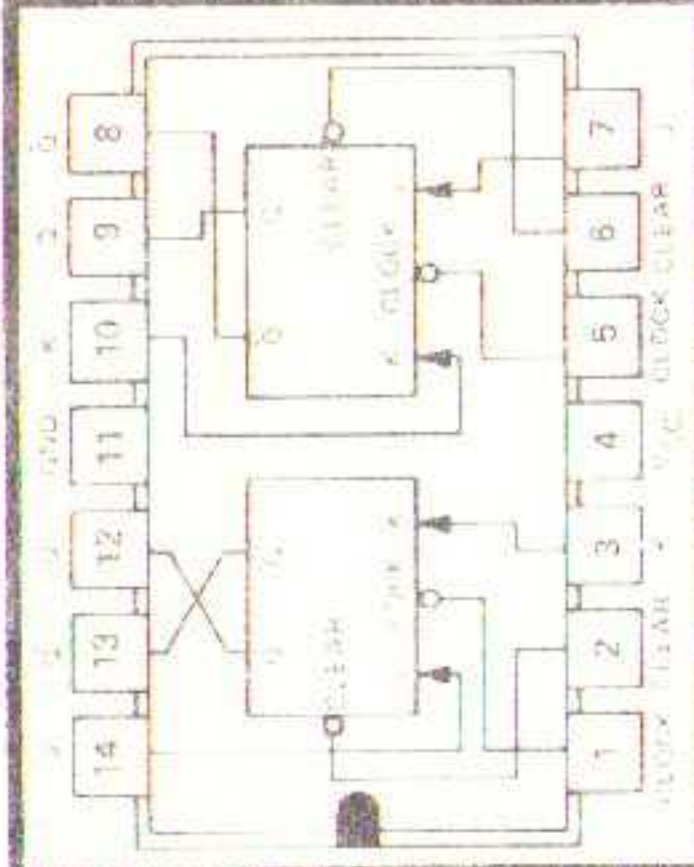
SN7473

DUAL J-K MASTER-SLAVE FLIP-FLOPS

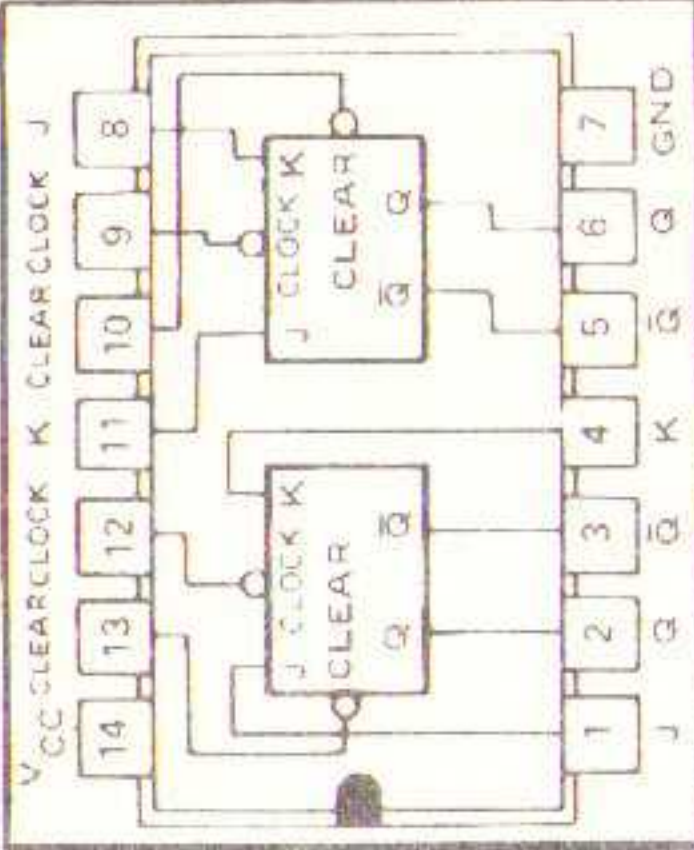
SN5473, SN7473
S FLAT PACKAGE
(TOP VIEW)



SN5473, SN7473
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN54107, SN74107
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to clear sets Q to logical 0
Clear is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: (See waveform on page 2-26)

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

logic

TRUTH TABLE (Each Flip-Flop)					
J	K	Q	Q _n	t _n	t _{n+1}
0	0	0	0	0	0
0	1	0	0	0	0
1	0	1	1	0	1
1	1	1	0	1	0

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

recommended operating conditions

Supply Voltage V_{CC} :	SN5473, SN54107 Circuits	SN7473, SN74107 Circuits
Operating Free-Air Temperature Range, T_A :	SN5473, SN54107 Circuits	SN7473, SN74107 Circuits
Normalized Fan-Out From Each Output, N		
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 69)		
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 70)		
Input Setup Time, t_{setup} (See Figure 69)		
Input Hold Time, t_{hold}		

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
-55	25	125	°C
0	25	70	°C
20		10	ns
25			ns
≥ t _{p(clock)}			
0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{in} (1) Input voltage required to ensure logical 1 at any input terminal	46 and 47	V _{CC} = MIN	2			V
V _{in} (0) Input voltage required to ensure logical 0 at any input terminal	46 and 47	V _{CC} = MIN		0.8		V
V _{out} (1) Logical 1 output voltage	46	V _{CC} = MIN, I _{load} = -400 µA	2.4	3.5		V
V _{out} (0) Logical 0 output voltage	47	V _{CC} = MIN, I _{sink} = 16 mA	0.22	0.4		V
I _{in} (0) Logical 0 level input current at J or K	48	V _{CC} = MAX, V _{in} = 0.4 V		-1.6		mA
I _{in} (0) Logical 0 level input current at clear or clock	48	V _{CC} = MAX, V _{in} = 0.4 V		-3.2		mA
I _{in} (1) Logical 1 level input current at J or K	49	V _{CC} = MAX, V _{in} = 2.4 V		40		µA
I _{in} (1) Logical 1 level input current at clear or clock	49	V _{CC} = MAX, V _{in} = 2.4 V		1		mA
I _{OS} Short-circuit output current§	50	V _{CC} = MAX, V _{in} = 0	-20		-57	mA
I _{CC} Supply current	49	V _{CC} = MAX, V _{in} = 5 V	-18	20	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

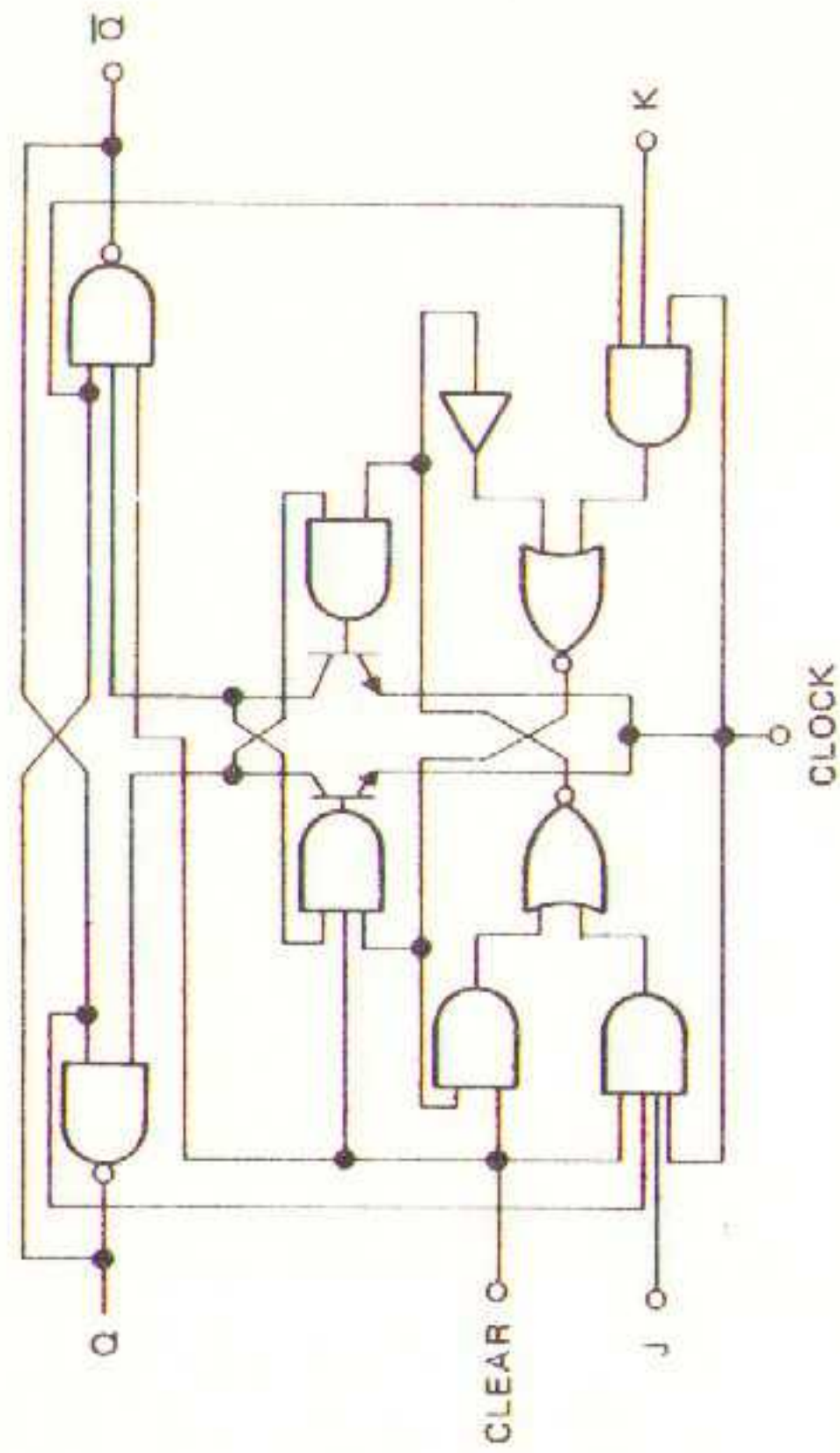
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

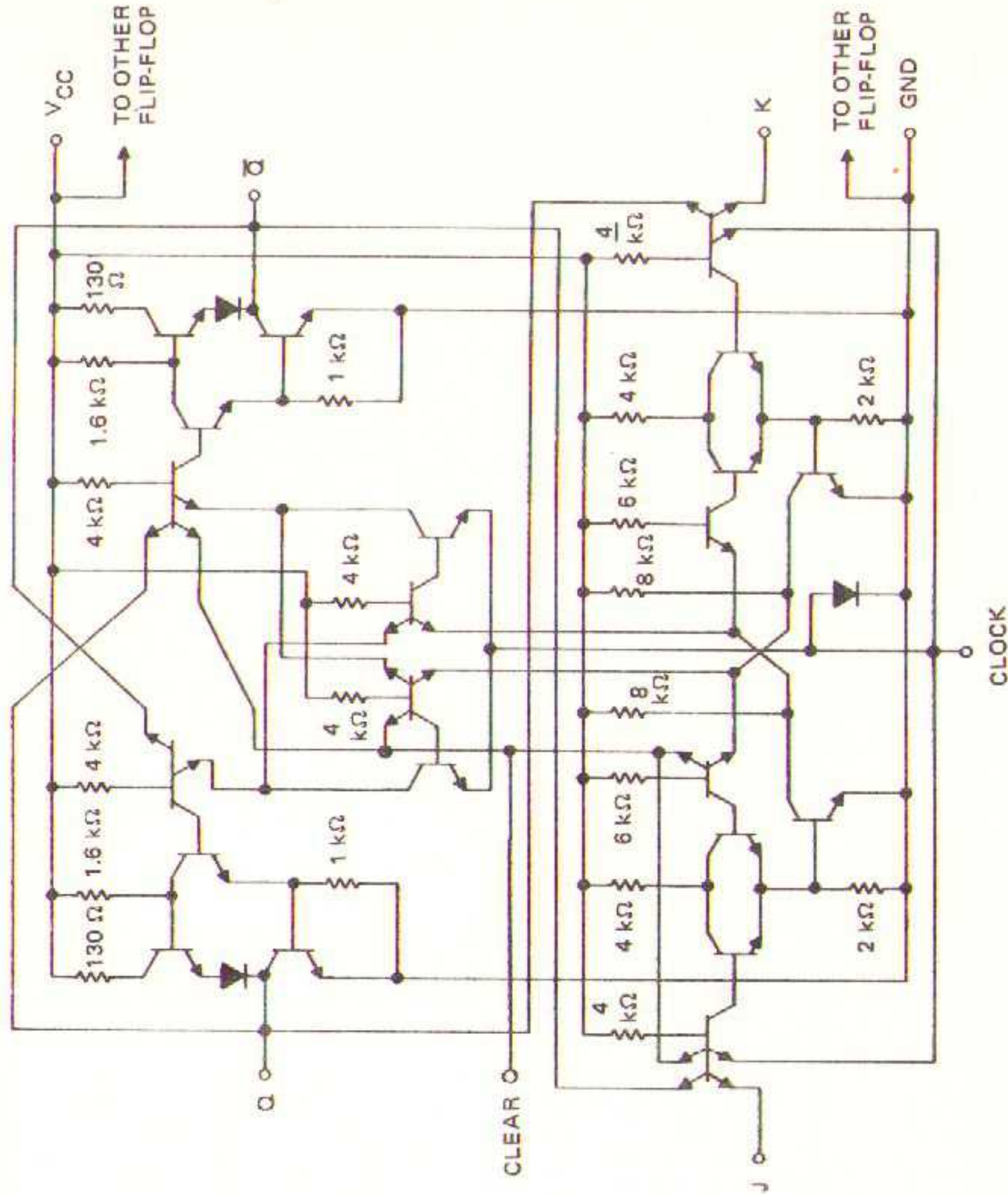
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{clock} Maximum clock frequency	69	C _L = 15 pF, R _L = 400 Ω	15	20		MHz
t _{pd1} Propagation delay time to logical 1 level from clear to output	70	C _L = 15 pF, R _L = 400 Ω		16	25	ns
t _{pd0} Propagation delay time to logical 0 level from clear to output	70	C _L = 15 pF, R _L = 400 Ω		25	40	ns
t _{pd1} Propagation delay time to logical 1 level from clock to output	69	C _L = 15 pF, R _L = 400 Ω	10	16	25	ns
t _{pd0} Propagation delay time to logical 0 level from clock to output	69	C _L = 15 pF, R _L = 400 Ω	10	25	40	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

logic

TRUTH TABLE (Each Flip-Flop)

INPUT	D	t _{nt} -1	
		OUTPUT Q	OUTPUT $\bar{Q}$
0	0	0	1
1	1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

description

These monolithic, dual, D-type, edge-triggered flip-flops feature direct clear and preset inputs and complementary Q and $\bar{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

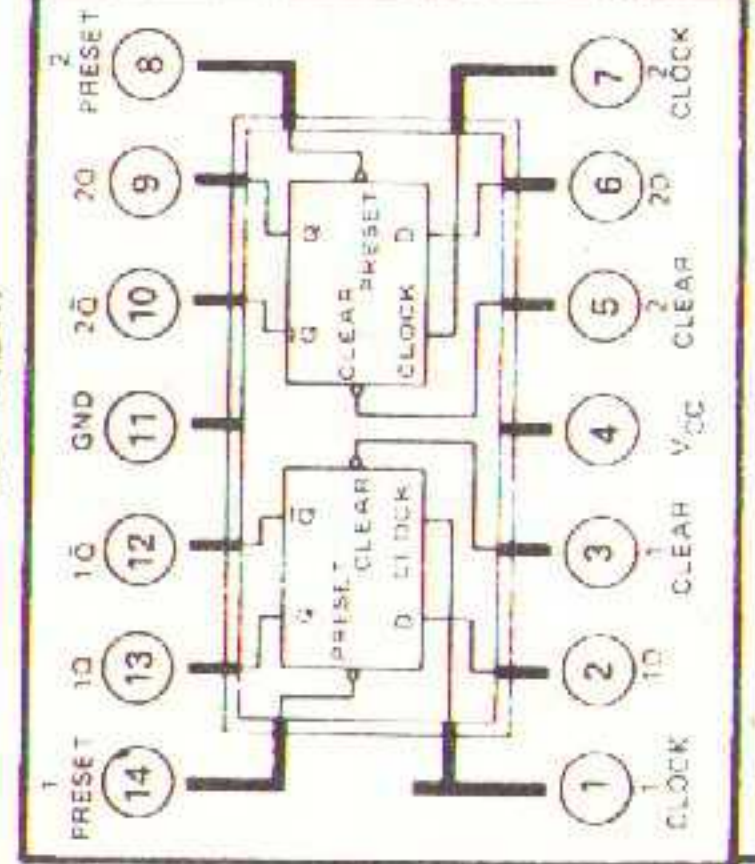
Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

These dual flip-flops have the same clocking characteristics as the SN5470/SN7470 gated (edge-triggered) flip-flop circuits, and both are ideally suited for medium- to-high-speed applications. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

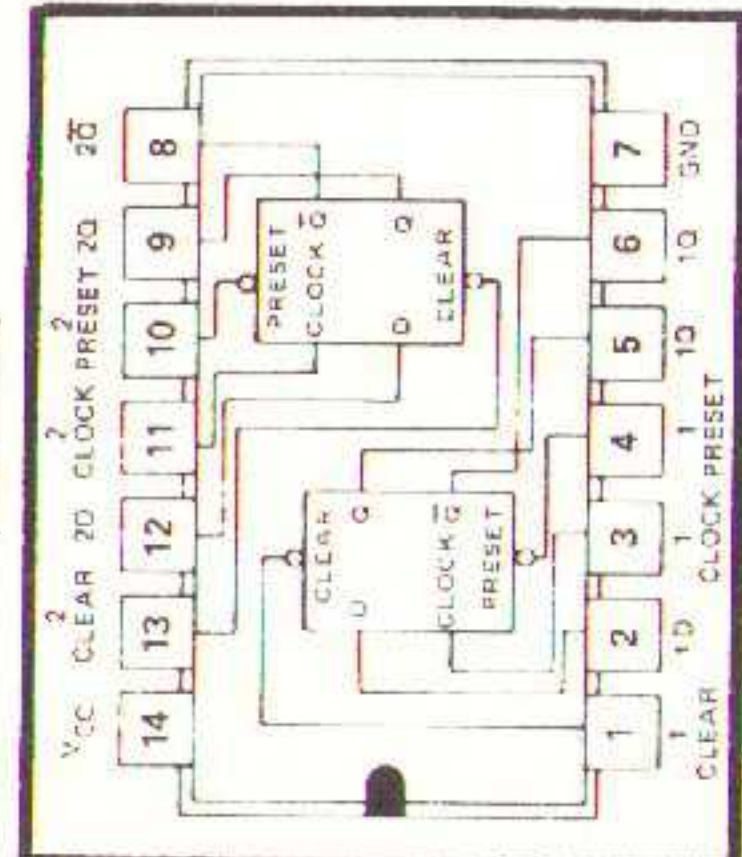
recommended operating conditions

Supply Voltage V _{CC} :	SN5474 Circuits	MIN	NOM	MAX	UNIT
	SN7474 Circuits	4.5	5	5.5	V
Operating Free-Air Temperature Range, T _A :	SN5474 Circuits	4.75	5	5.25	V
	SN7474 Circuits	-55	25	125	°C
Normalized Fan-Out From Each Output, N:		0	25	70	°C
Width of Clock Pulse, t _p (clock) (See figure 71)		30		10	ns
Width of Preset Pulse, t _p (preset) (See figure 67)		30			ns
Width of Clear Pulse, t _p (clear) (See figure 67)		30			ns

S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{in} (1) Input voltage required to ensure logical 1 at any input terminal	52 and 53	V _{CC} = MIN	2			V
V _{in} (0) Input voltage required to ensure logical 0 at any input terminal	52 and 53	V _{CC} = MIN		0.8		V
V _{out} (1) Logical 1 output voltage	52	V _{CC} = MIN, I _{load} = -400 μA	2.4	3.5		V
V _{out} (0) Logical 0 output voltage	53	V _{CC} = MIN, I _{sink} = 16 mA		0.22	0.4	V
I _{in} (0) Logical 0 level input current at preset or D	54	V _{CC} = MAX, V _{in} = 0.4 V		-1.6		mA
I _{in} (0) Logical 0 level input current at clear or clock	54	V _{CC} = MAX, V _{in} = 0.4 V		-3.2		mA
I _{in} (1) Logical 1 level input current at D	55	V _{CC} = MAX, V _{in} = 2.4 V		40		μA
I _{in} (1) Logical 1 level input current at preset or clock	55	V _{CC} = MAX, V _{in} = 5.5 V		1		mA
I _{in} (1) Logical 1 level input current at clear	55	V _{CC} = MAX, V _{in} = 2.4 V		80		μA
I _{OS} Short-circuit output current‡	56	V _{CC} = MAX, V _{in} = 0	-20		-57	mA
I _{CC} Supply current	55	V _{CC} = MAX, V _{in} = 5 V	-18		-30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

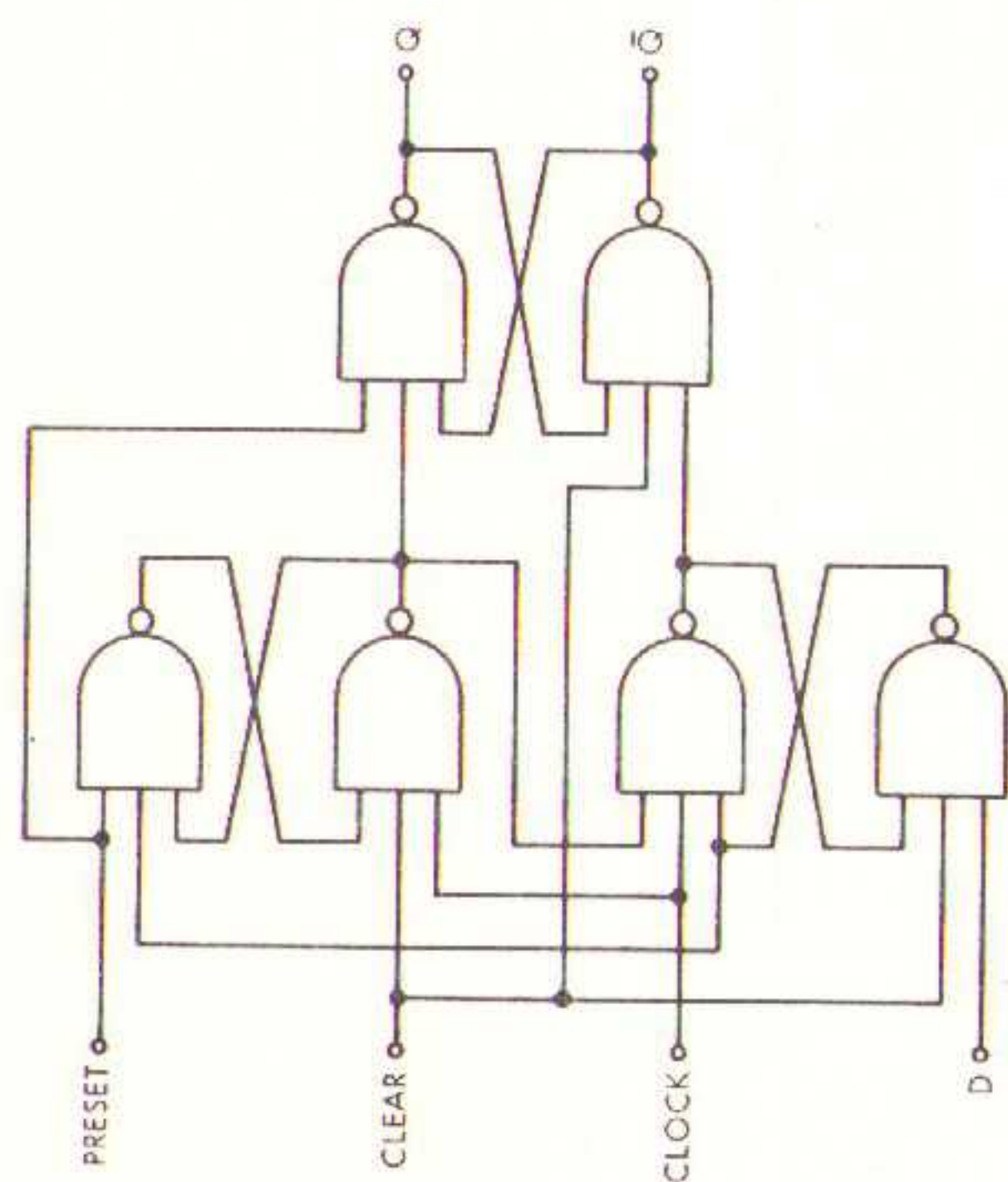
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

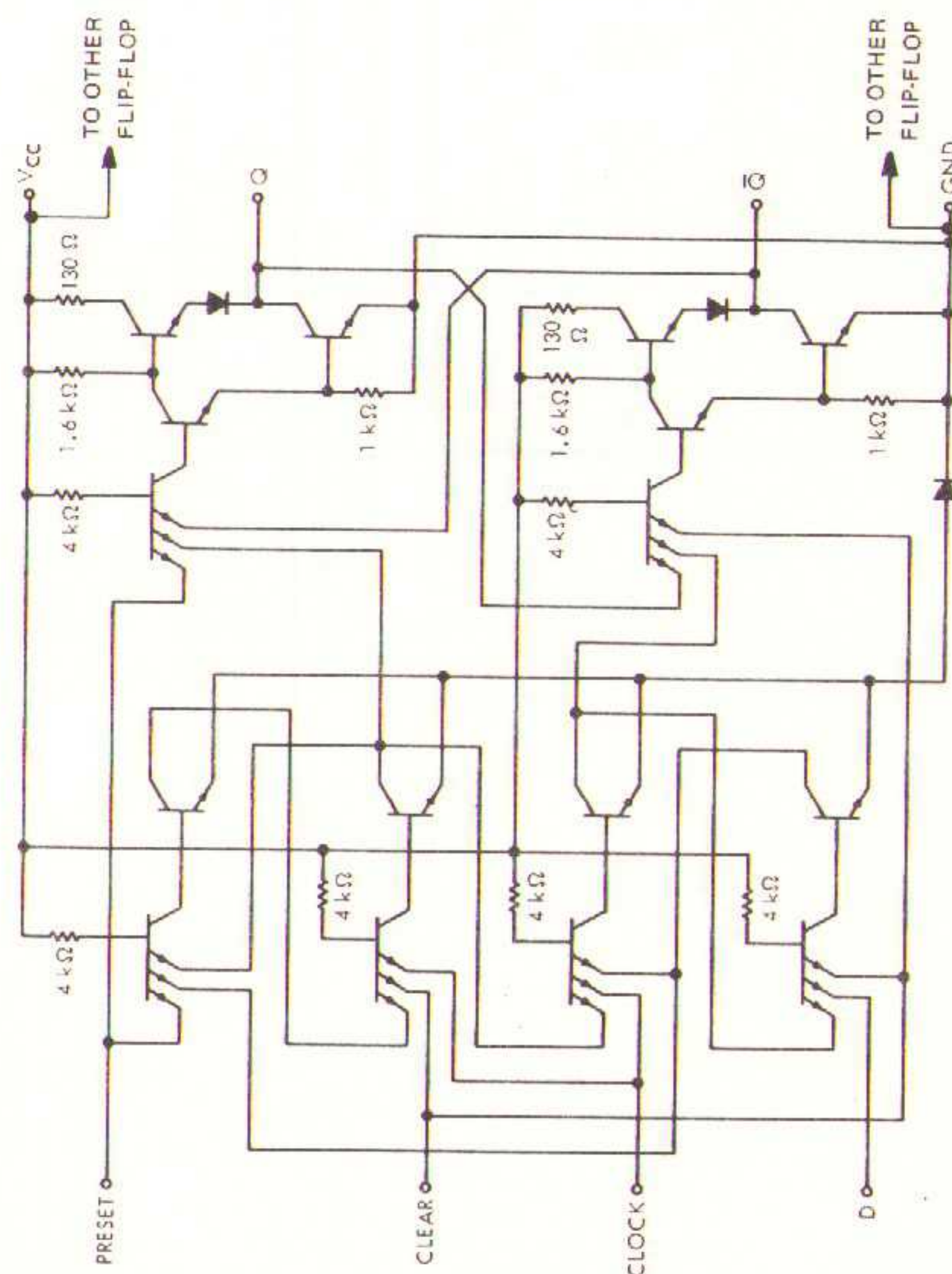
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{clock} Maximum clock frequency	71	C _L = 15 pF, R _L = 400 Ω	15	25		MHz
t _{setup} Minimum input setup time	71	C _L = 15 pF, R _L = 400 Ω		15	20	ns
t _{hold} Minimum input hold time	71	C _L = 15 pF, R _L = 400 Ω		2	5	ns
t _{pd1} Propagation delay time to logical 1 level from clear or preset to output	67	C _L = 15 pF, R _L = 400 Ω			25	ns
t _{pd0} Propagation delay time to logical 0 level from clear or preset to output	67	C _L = 15 pF, R _L = 400 Ω			40	ns
t _{pd1} Propagation delay time to logical 1 level from clock to output	71	C _L = 15 pF, R _L = 400 Ω	10	14	25	ns
t _{pd0} Propagation delay time to logical 0 level from clock to output	71	C _L = 15 pF, R _L = 400 Ω	10	20	40	ns

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functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

SN7475 SN74100

8-BIT AND 4-BIT BISTABLE LATCHES

TRUTH TABLE (Each Latch)

t_n	t_{n+1}	Q
D	Q	1
0	0	0

logic

NOTES: 1. t_n = bit time before clock pulse transition.
2. t_{n+1} = bit time after clock pulse transition.
NC—No Internal Connection

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

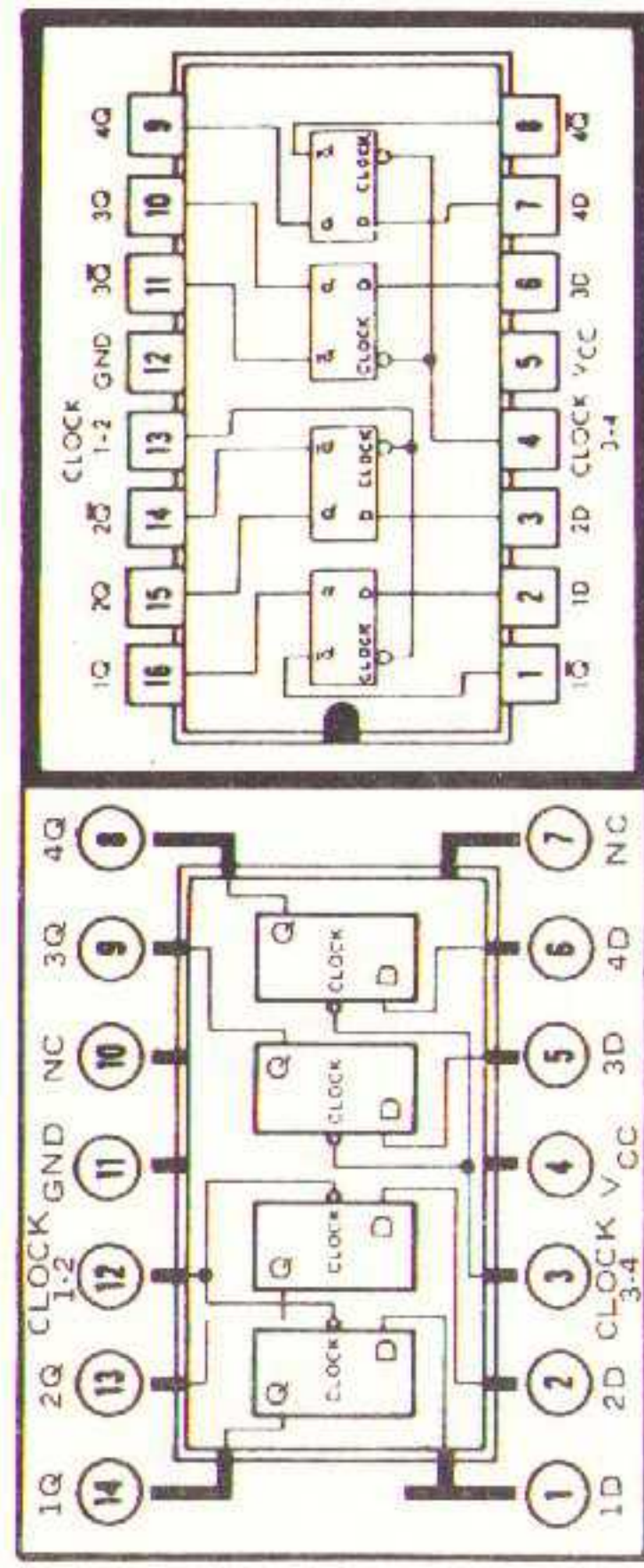
The SN5475/SN7475 features complementary Q and $\bar{Q}$ outputs from a 4-bit latch, and is available in the 16-pin packages. For higher component density applications the SN5477/SN7477 4-bit latch is available in the 14-pin flat package. The SN54100/SN74100 features two independent quadruple latches in a single 24-pin dual-in-line package. These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of -55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

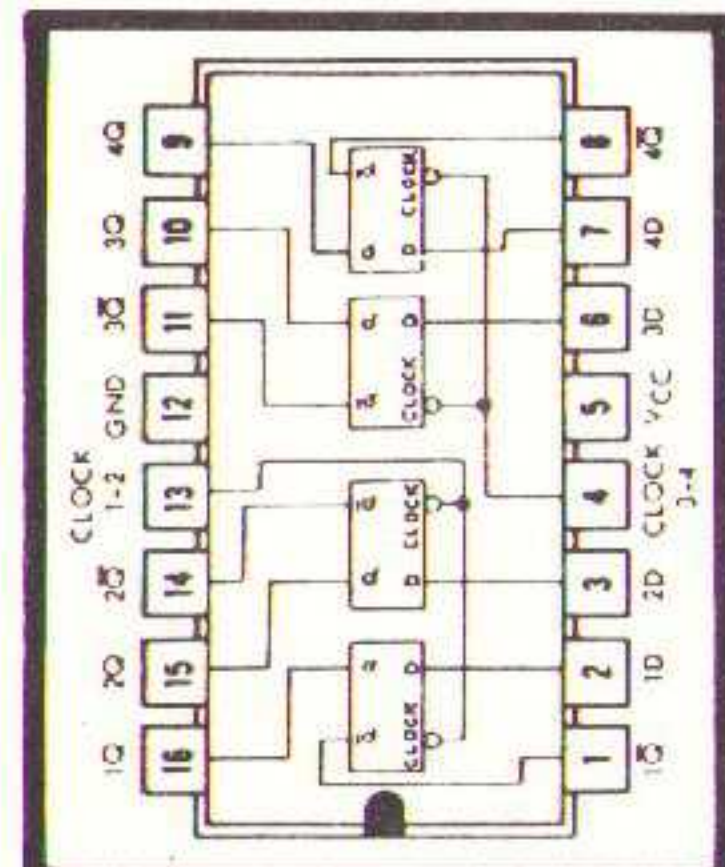
Supply Voltage, VCC (See Note 3)	7 V
Input Voltage, V_{in} (See Notes 3 and 4)	5.5 V
Operating Case Temperature Range: SN5477S	-55°C to 125°C
Operating Free-Air Temperature Range: SN5475J/N, SN54100N	-55°C to 125°C
SN7475J/N, SN74100N	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

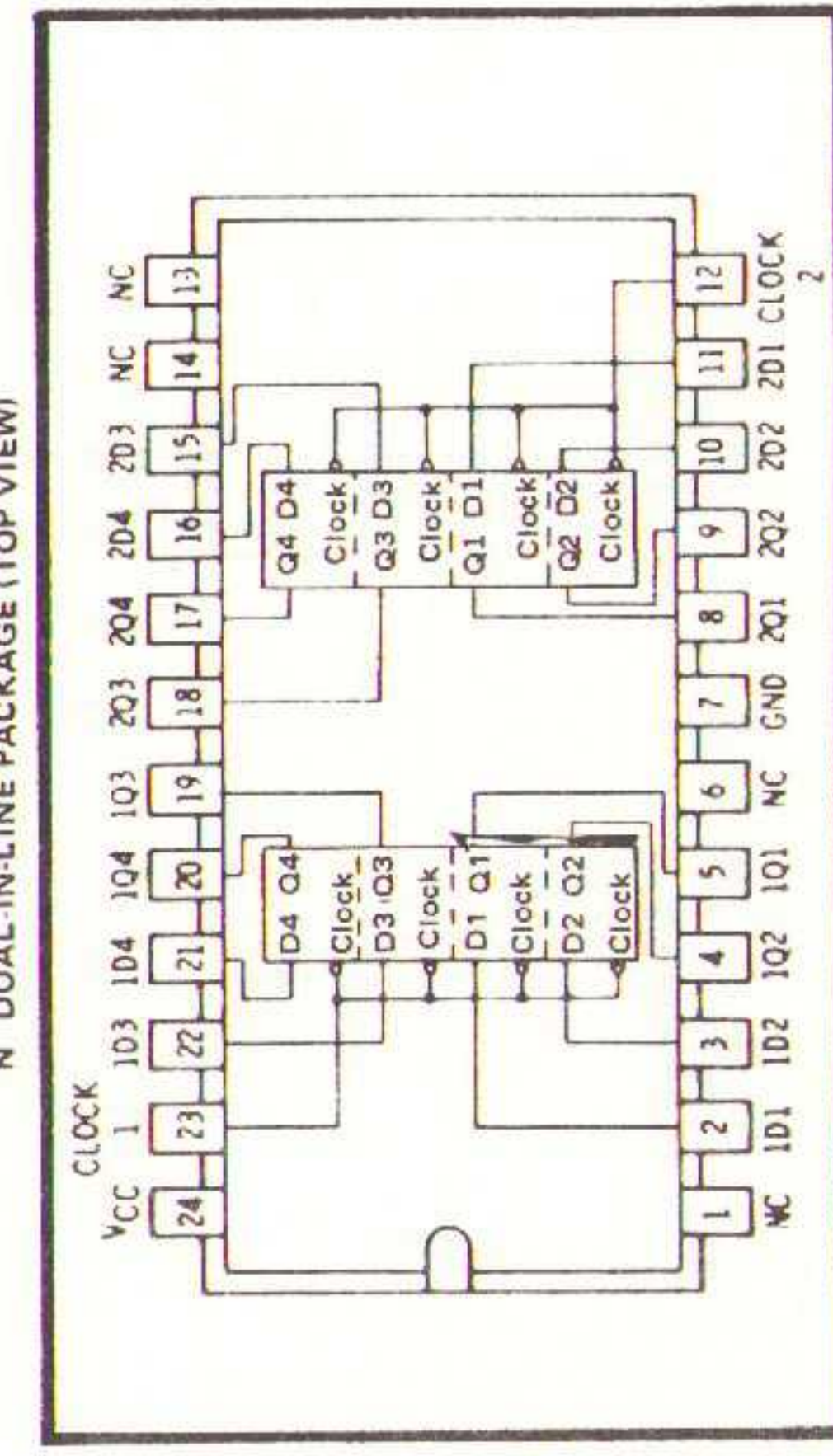
SN5477/SN7477
S FLAT PACKAGE
(TOP VIEW)



SN5475/SN7475
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN54100/SN74100
N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

recommended operating conditions (over operating temperature range)

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
		10	

Supply Voltage VCC (See Note 3): SN5475, SN5477, SN54100

Normalized Fan-Out From Outputs SN7475, SN7477, SN74100

NOTE: 3. These voltages are with respect to network ground terminal.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in}(1)$	1	VCC = MIN	2			V
$V_{in}(0)$	2	VCC = MIN			0.8	V
$V_{out}(1)$	1 and 2	VCC = MIN, $I_{load} = -400 \mu A$	2.4			V
$V_{out}(0)$	1 and 2	VCC = MIN, $I_{sink} = 16 mA$			0.4	V
$I_{in}(0)$	3	VCC = MAX, $V_{in} = 0.4 V$			-3.2	mA
$I_{in}(0)$	3	VCC = MAX, SN5475, SN5477, SN7475, SN7477			-6.4	mA
$I_{in}(0)$	3	VCC = MAX, SN54100, SN74100			-12.8	mA
$I_{in}(1)$	3	VCC = MAX, $V_{in} = 2.4 V$			80	μA
$I_{in}(1)$	3	VCC = MAX, $V_{in} = 5.5 V$			1	mA
$I_{in}(1)$	3	VCC = MAX, SN5475, SN5477, SN7475, SN7477			160	μA
$I_{in}(1)$	3	VCC = MAX, SN54100, SN74100			320	μA
I_{OS}	4	VCC = MAX, $V_{in} = 5.5 V$			1	mA
I_{OS}	4	VCC = MAX, SN5475, SN5477, SN54100			-57	mA
I_{OS}	4	VCC = MAX, $V_{out} = 0$			-18	mA
I_{OS}	4	VCC = MAX, SN7475, SN7477, SN74100			-57	mA
I_{OS}	4	VCC = MAX, SN5475, SN5477			32	mA
I_{OS}	4	VCC = MAX, SN54100			64	mA
I_{OS}	4	VCC = MAX, SN7475, SN7477			32	mA
I_{OS}	4	VCC = MAX, SN74100			64	mA
I_{OS}	4	VCC = MAX, SN5475, SN5477, SN54100			106	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at VCC = 5 V, TA = 25°C.

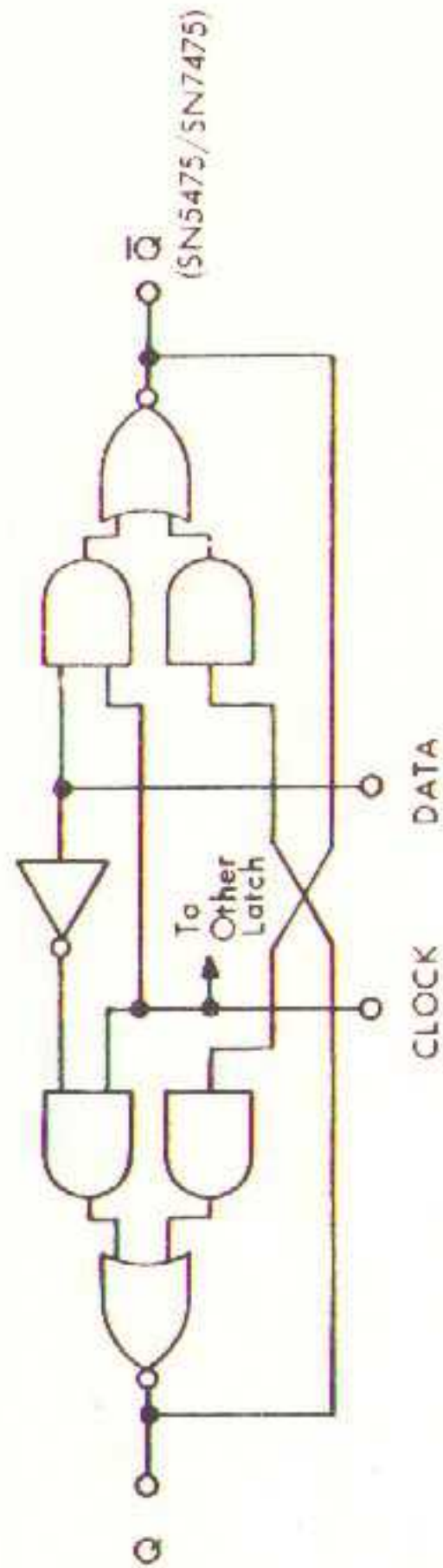
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

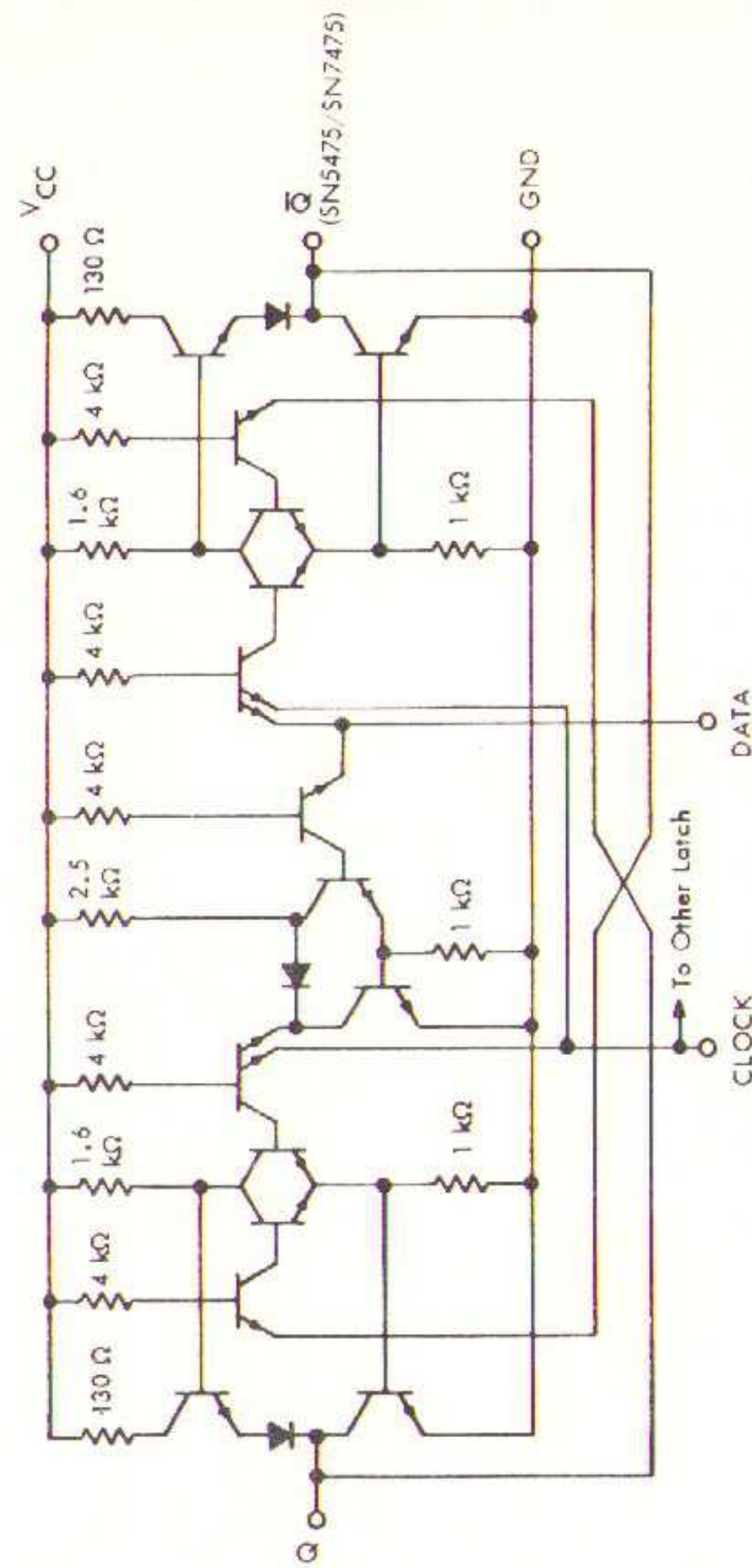
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup1}	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		7	20	ns
t_{setup0}	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		14	20	ns
t_{hold1}	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$	0	15 [†]		ns
t_{hold0}	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$	0	6 [†]		ns
$t_{\text{pd1(D-Q)}}$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		16	30	ns
$t_{\text{pd0(D-Q)}}$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		14	25	ns
$t_{\text{pd1(D-Q)}}^*$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		24	40	ns
$t_{\text{pd0(D-Q)}}^*$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		7	15	ns
$t_{\text{pd1(C-Q)}}$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		16	30	ns
$t_{\text{pd0(C-Q)}}$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		7	15	ns
$t_{\text{pd1(C-Q)}}^*$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		16	30	ns
$t_{\text{pd0(C-Q)}}^*$	6	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		7	15	ns

* These typical times indicate that period occurring prior to the fall of clock pulse (t_{Q}) below 1.5 V when data at the D input will still be recognized and stored.

functional block diagram (each latch)



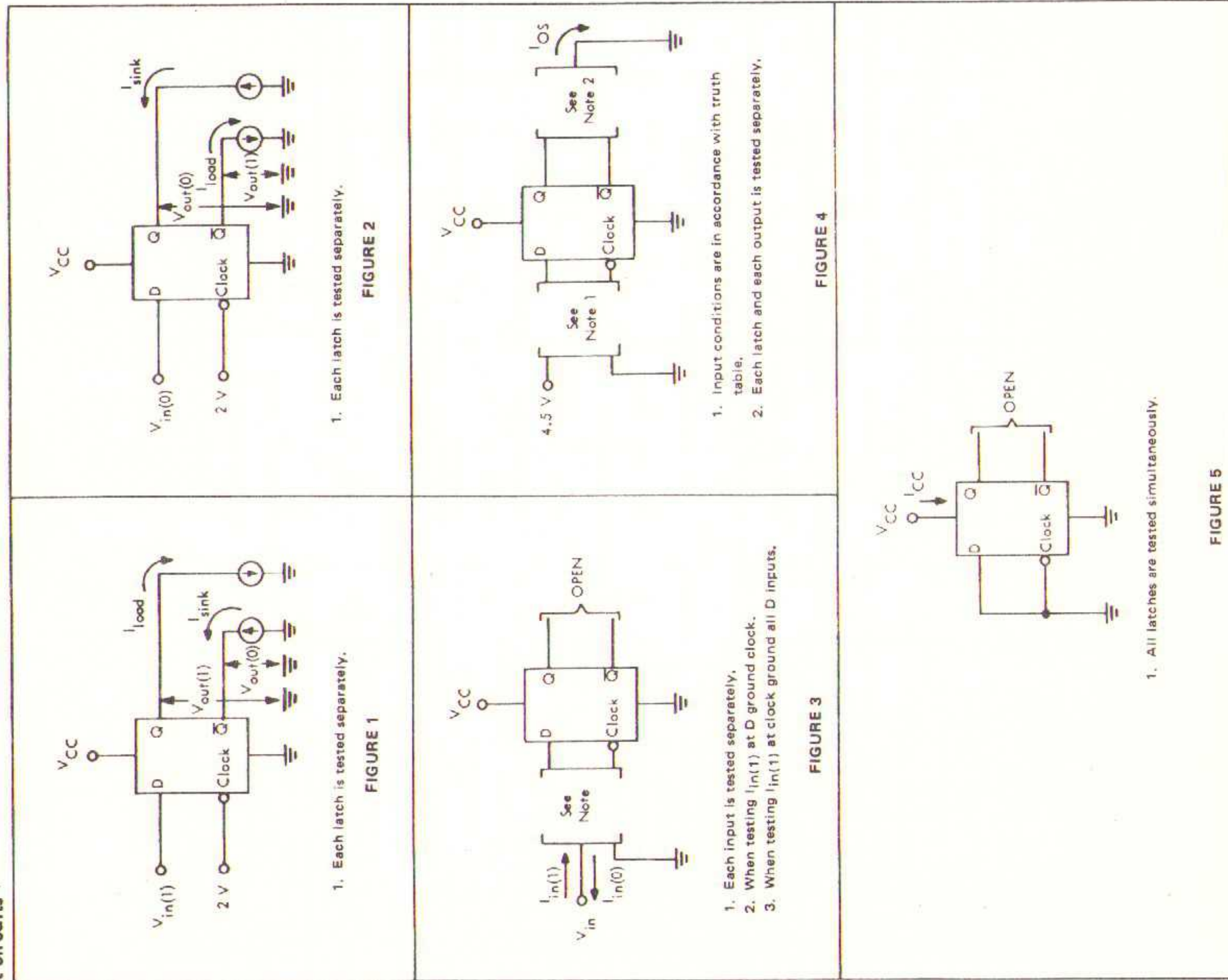
schematic (each latch)



Component values shown are nominal.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



† Arrows indicate actual direction of current flow. Complementary $\bar{Q}$ outputs are available on the SN5475/SN7475.

PARAMETER MEASUREMENT INFORMATION

switching characteristics †

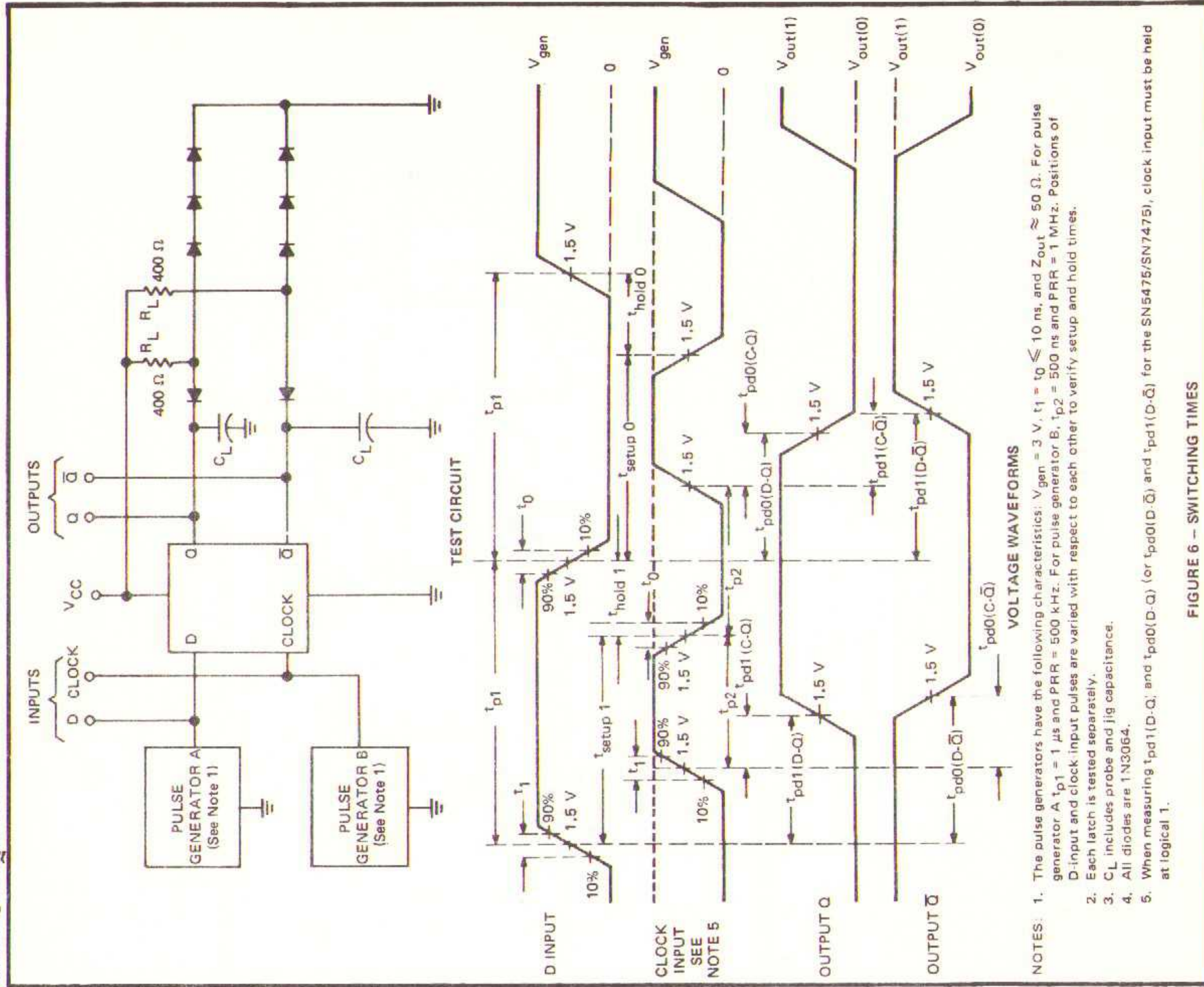


FIGURE 6 — SWITCHING TIMES

† Complementary $\bar{Q}$ outputs are on the SN5475/SN7475 only.

TYPICAL APPLICATION

temporary storage of binary data

This application demonstrates the use of the SN7475 bistable latch as a temporary storage of binary-coded decimal data, from the SN7490 decade counter, which is to be decoded by the SN7441 decoder/driver. Temporary storage is desirable at this point for two reasons:

- At counting frequencies above several cycles per second, it is sometimes desirable to eliminate the flicker on the display tube caused by reading an input count which is too fast to be recognized.
- During the time that the latch is storing information the decade counter may start acquiring data for the next display.

A typical sequence of operation is illustrated (see Figure 7):

- During t_1 , reset decade counter to 0. At end of t_1 , indicator will display "0".
- During t_2 , count BCD 3 at output of SN7490. Indicator still displays "0".
- At start of t_3 , indicator will display "3". At end of t_3 , BCD 3 is committed to memory by SN7475 and the SN7490 may begin counting again.
- During t_4 , reset decade counter to 0 and count BCD 5 at output of SN7490. Indicator still displays "3".
- At start of t_5 , indicator will display "5". At end of t_5 , BCD 5 is committed to memory by SN7475 and the SN7490 is released.

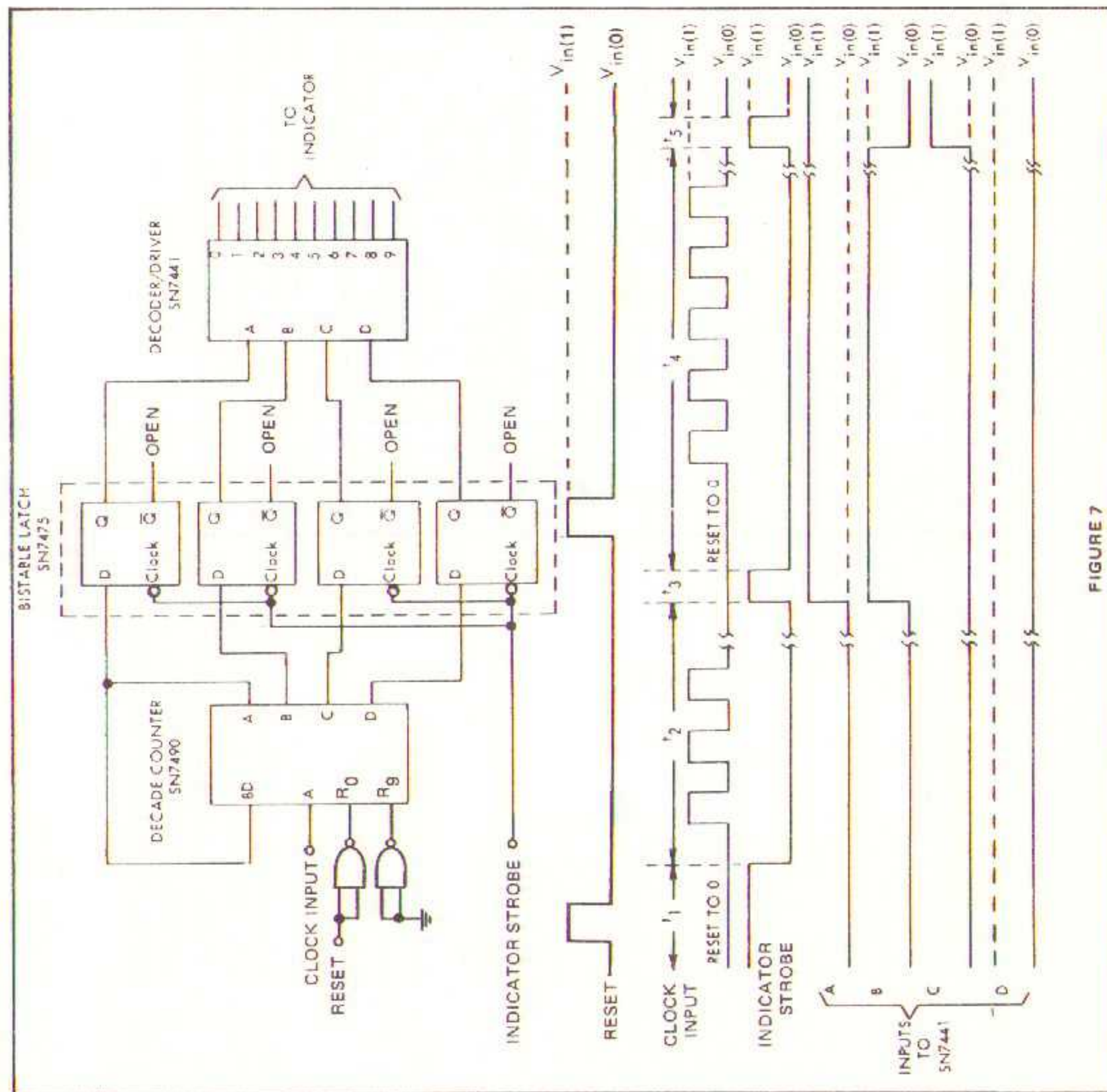


FIGURE 7

TYPICAL APPLICATION

dual D-type master-slave flip-flop

This application demonstrates the use of the SN7475 as a dual D-type master-slave flip-flop, provided that two-phase clocking is permissible. Each of the D-type flip-flops are formed by merely interconnecting the Q output of one of the latches (which serves as the master) to the data input of another latch (which serves as the slave). Each of these interconnected latches must have a separate clock line; therefore if a dual D-type master-slave flip-flop is constructed from a single package (see Figure 3) they must be operated synchronously.

A typical transfer of data is illustrated. Note that after the start of t_1 the data input is released to acquire new information as the master section has "locked up" the original data after clock pulse A_1 . At the start of t_2 the data "locked up" in the master is transferred to the output, and at the end of t_2 (and for the duration of t_3) the slave retains the original data.

This type of flip-flop is desirable in applications where speed is not a primary requirement and where the additional clock skew, resulting from this delay between the two clock pulses, affords greater system reliability.

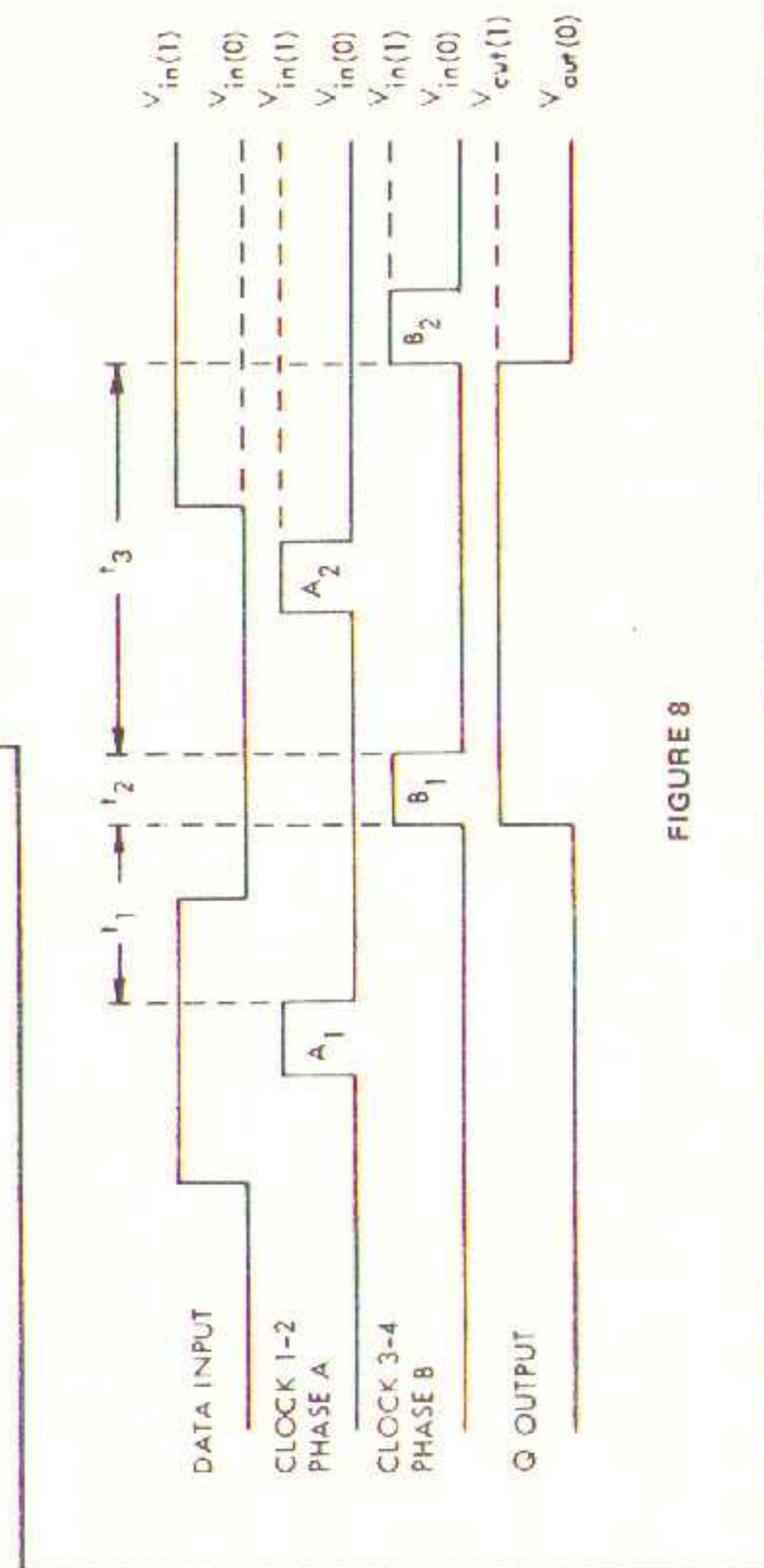


FIGURE 8

logic

TRUTH TABLE (Each Flip-Flop)			
t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q _n	Q _n
0	1	0	1
1	0	1	0
1	1	Q _n	Q _n

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

description

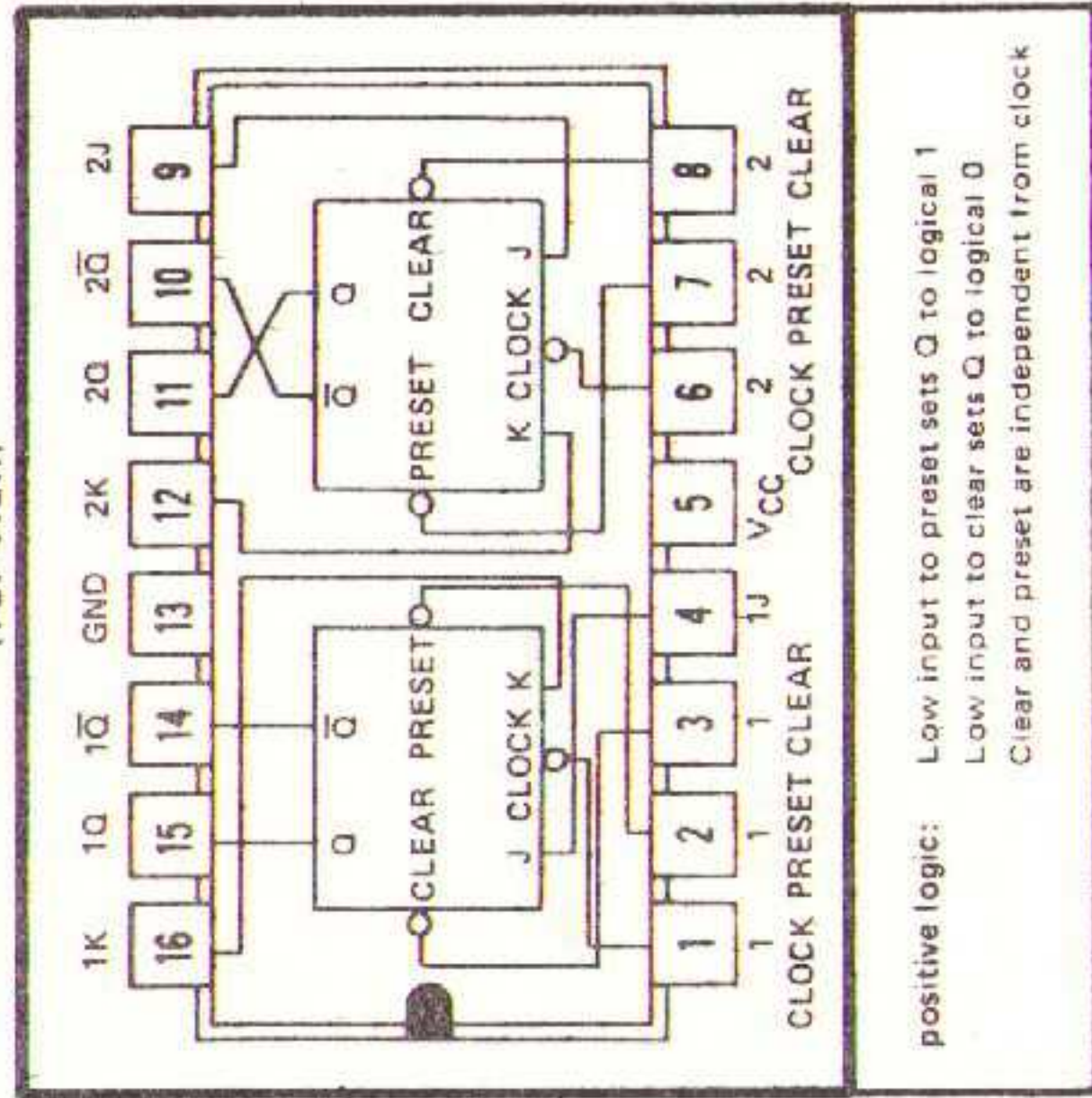
The SN7476 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

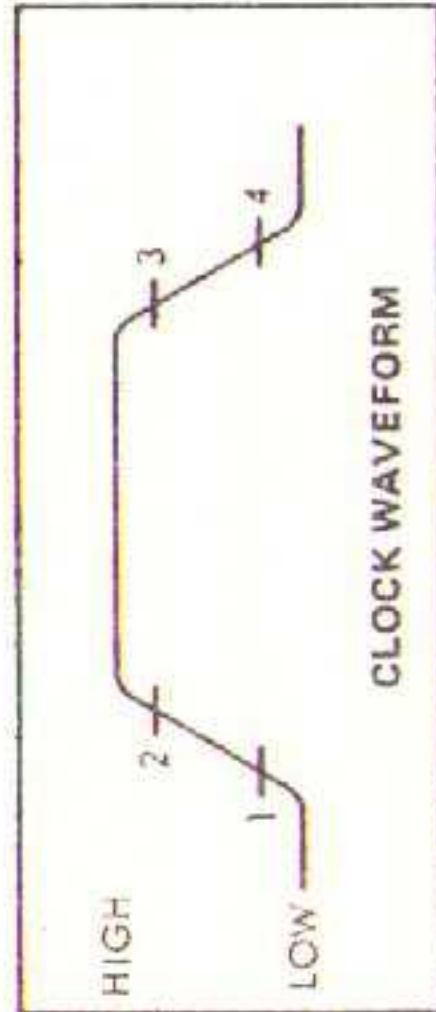
recommended operating conditions

Supply Voltage V _{CC} :	SN5476 Circuits	SN7476 Circuits	Operating Free-Air Temperature Range, T _A :	SN5476 Circuits	SN7476 Circuits	Normalized Fan-Out From Each Output, N:	Width of Clock Pulse, t _{p(clock)} (See figure 69):	Width of Preset Pulse, t _{p(preset)} (See figure 70):	Width of Clear Pulse, t _{p(clear)} (See figure 70):	Input Setup Time, t _{setup} (See figure 69):	Input Hold Time, t _{hold}
	4.5	4.75	-55	0	20	25	25	25	25	25	25
	5.5	5.25	125	70	10	10	10	10	10	10	10
	V	V	°C	°C	ns	ns	ns	ns	ns	ns	ns

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent from clock



switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

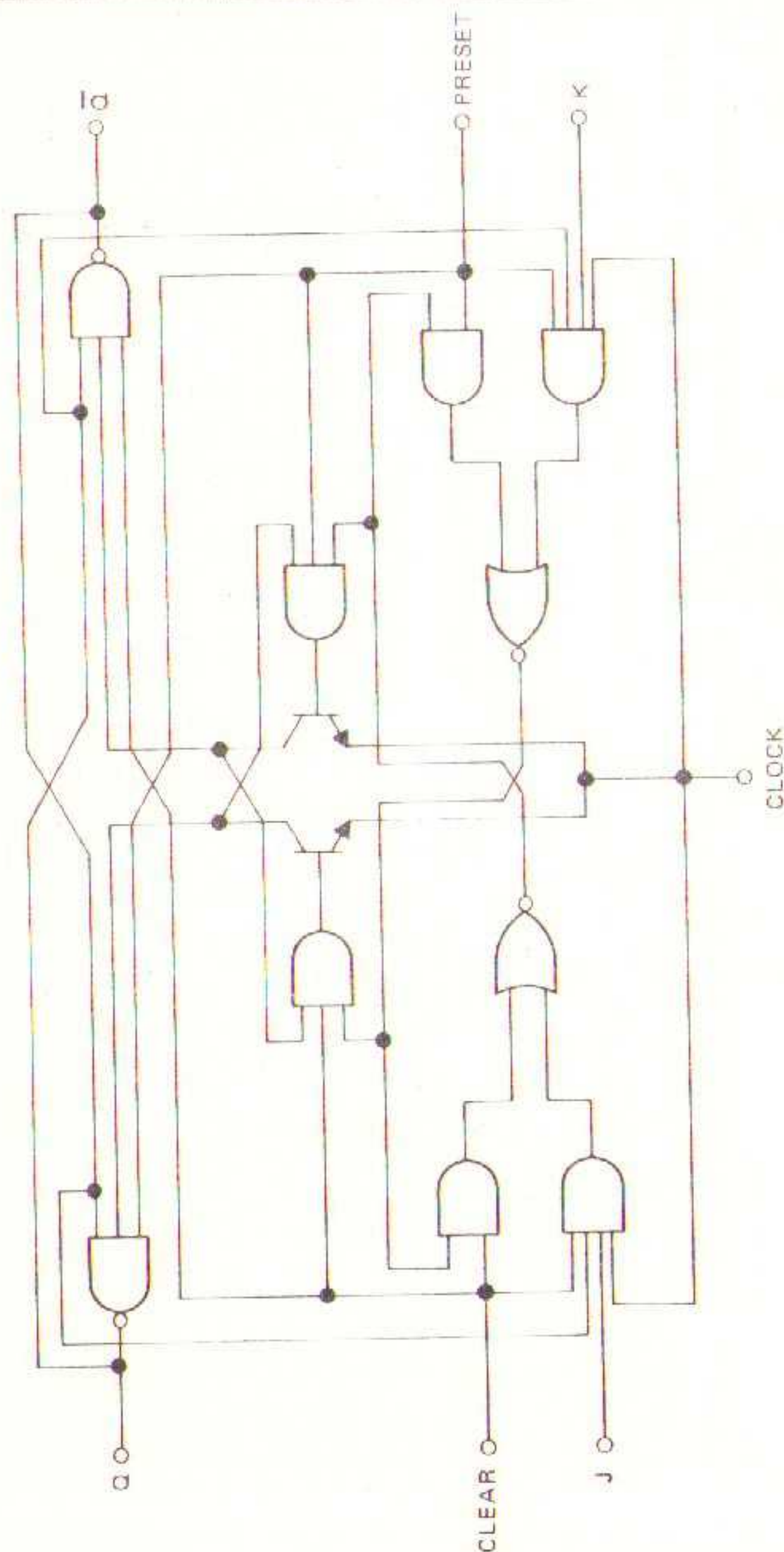
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{clock}	69	C _L = 15 pF, R _L = 400 Ω	15	20		MHz
t _{pd1}	70	C _L = 15 pF, R _L = 400 Ω		16	25	ns
t _{pd0}	70	C _L = 15 pF, R _L = 400 Ω		25	40	ns
t _{pd1}	69	C _L = 15 pF, R _L = 400 Ω	10	16	25	ns
t _{pd0}	69	C _L = 15 pF, R _L = 400 Ω	10	25	40	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

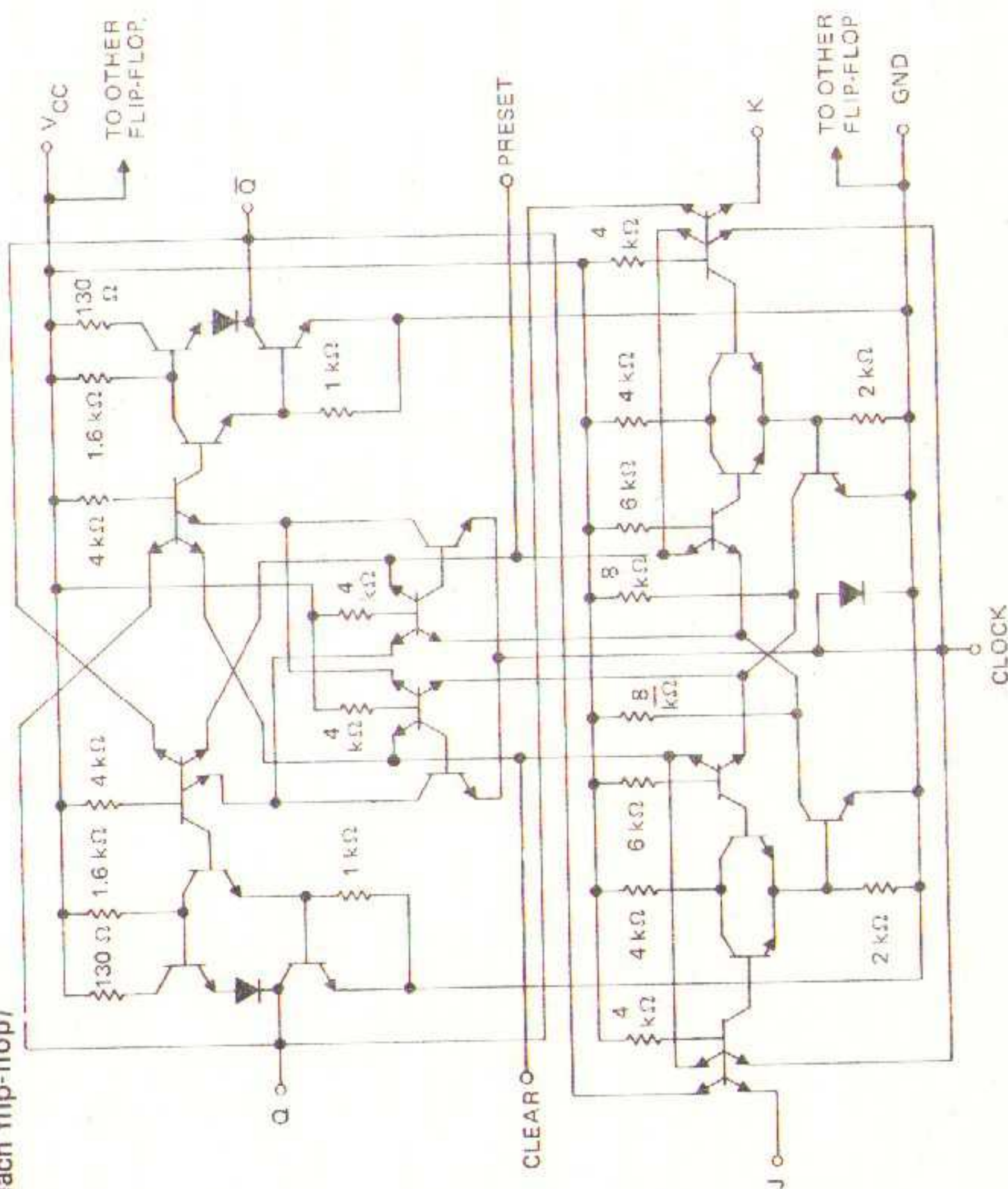
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

logic

TRUTH TABLE
(See Notes 1, 2, and 3)

C_n	B	A	C_{n+1}	Σ
0	0	0	1	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

NOTES: 1. $A = A^* \cdot A_1$, $B = B^* \cdot B_1$ where $A^* = A_1 \cdot A_2$, $B^* = B_1 \cdot B_2$.
2. When A^* or B^* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* respectively must be open or used to perform Dot-OR logic.

description

This single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ) and carry (C_{n+1}) outputs and inverted carry output is designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications. The circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4)	7 V
Input Voltage V_{in} (See Notes 4 and 5)	5.5 V
Operating Case Temperature Range	-55°C to 125°C
Operating Free-Air Temperature Range	-55°C to 125°C
Storage Temperature Range	0°C to 70°C
	-65°C to 150°C

recommended operating conditions (over operating temperature range)

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
		5	
		10	
		3	

NOTES: 4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

GATED FULL ADDERS

SN7480

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in}(1)$ Logical 1 input voltage	1 and 2	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Logical 0 input voltage	1 and 2	$V_{CC} = \text{MIN}$		0.8		V
$V_{out}(1)$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}$	2.4	3.5		V
$V_{out}(0)$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}$		0.22	0.4	V
Logical 0 level input current at A_1, A_2, B_1, B_2, A_C or B_C	3	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-1.6		mA
Logical 0 level input current at A^* or B^*	4	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-2.6		mA
Logical 0 level input current at C_n	4	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-8		mA
Logical 1 level input current at A_1, A_2, B_1, B_2, A_C or B_C	5	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$ $V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$		15	1	μA mA
Logical 1 level input current at C_n	6	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$ $V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$		200	1	μA mA
Short-circuit output current at Σ or Σ^*	7	$V_{CC} = \text{MAX}$	-20		-57	mA
Short-circuit output current at $\overline{\Sigma}$ or $\overline{\Sigma}^*$	7	$V_{CC} = \text{MAX}$	-18		-57	mA
Short-circuit output current at $\overline{C_{n+1}}$	7	$V_{CC} = \text{MAX}$	-20		-70	mA
Supply current	8	$V_{CC} = \text{MAX}$	-18		-70	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 9 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	1	$C_L = 15 \text{ pF}, R_L = 780 \Omega$		13	17	ns
t_{pd0}			2	$C_L = 15 \text{ pF}, R_L = 780 \Omega$		8	12	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	3	$C_L = 15 \text{ pF}, R_L = 780 \Omega$		18	25	ns
t_{pd0}			4	$C_L = 15 \text{ pF}, R_L = 780 \Omega$		38	55	ns
t_{pd1}	A_C	Σ	5	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		52	70	ns
t_{pd0}			6	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	7	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		38	55	ns
t_{pd0}			8	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		56	75	ns
t_{pd1}	A_1	A^*	9	$C_L = 15 \text{ pF}$		48	65	ns
t_{pd0}			10	$C_L = 15 \text{ pF}$		17	25	ns
t_{pd1}	B_1	B^*	11	$C_L = 15 \text{ pF}$		48	65	ns
t_{pd0}			12	$C_L = 15 \text{ pF}$		17	25	ns

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

TYPICAL APPLICATIONS

n-bit binary adder or subtractor (see figures A and B)

The SN7480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the C_{n+1} output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This

interconnection method is illustrated by bit 2 and bit 4 of the adder (Figure A). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

When performing subtraction (Figure B) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (Figure A), input control is applied to A_2 and B_2 of odd-numbered bits and to A_C and B_C of even-numbered bits. For the subtractor (Figure B), input control is applied to A_2 and B_C of the odd-numbered bits and to A_C and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.

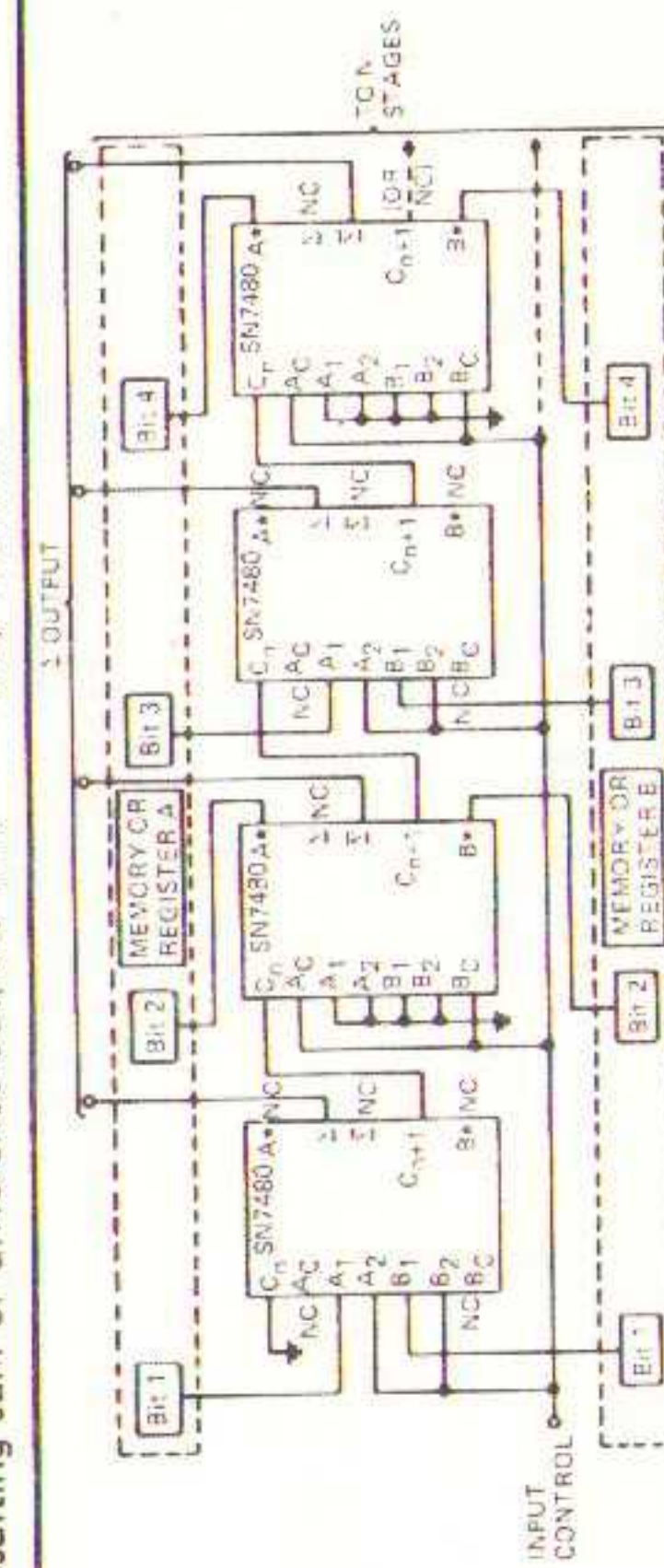


FIGURE A -- N-BIT BINARY ADDER

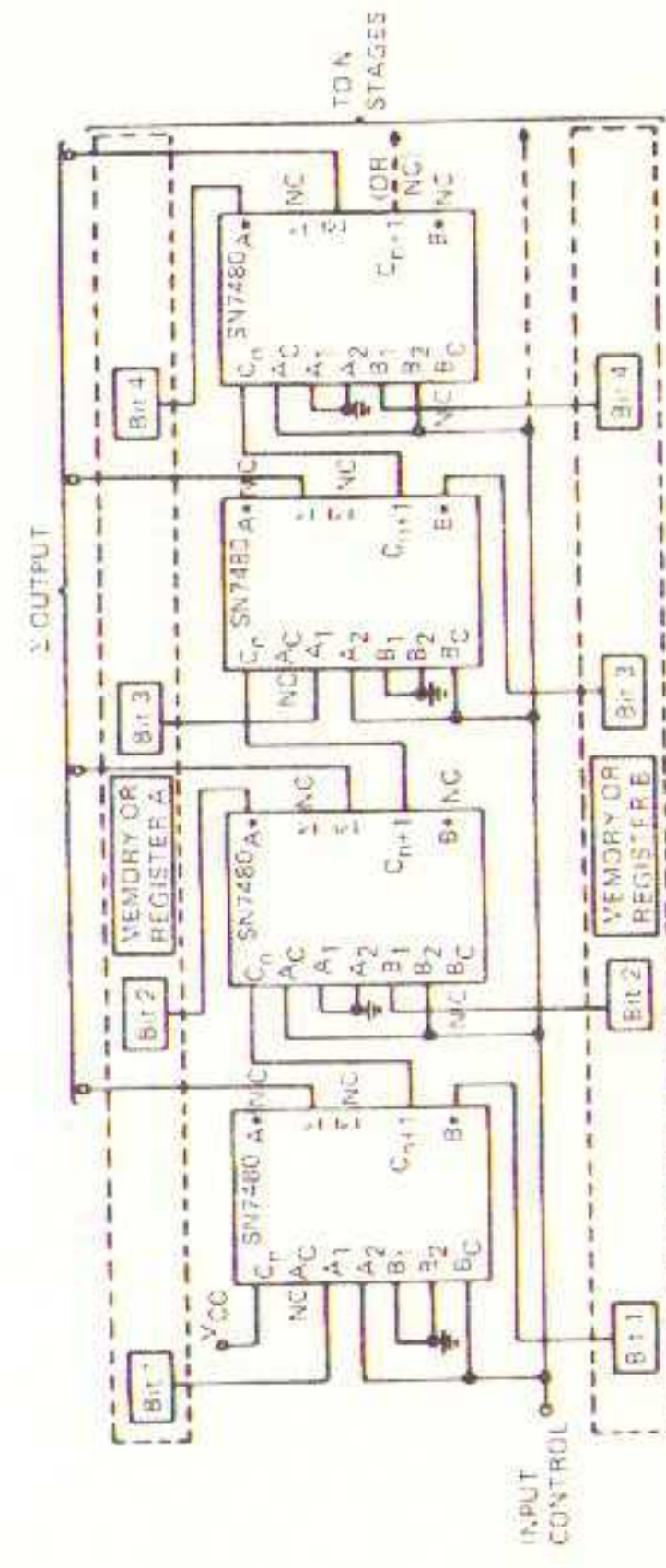


FIGURE B -- N-BIT BINARY SUBTRACTOR

NOTE: Functions noted as NC are open.

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure C)

This application fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A1 and B1, and externally by a type SN7405 TTL gate for registers A2 and B2. Dot-OR logic is performed at the A* and B* nodes within the adder when the register selection is made.

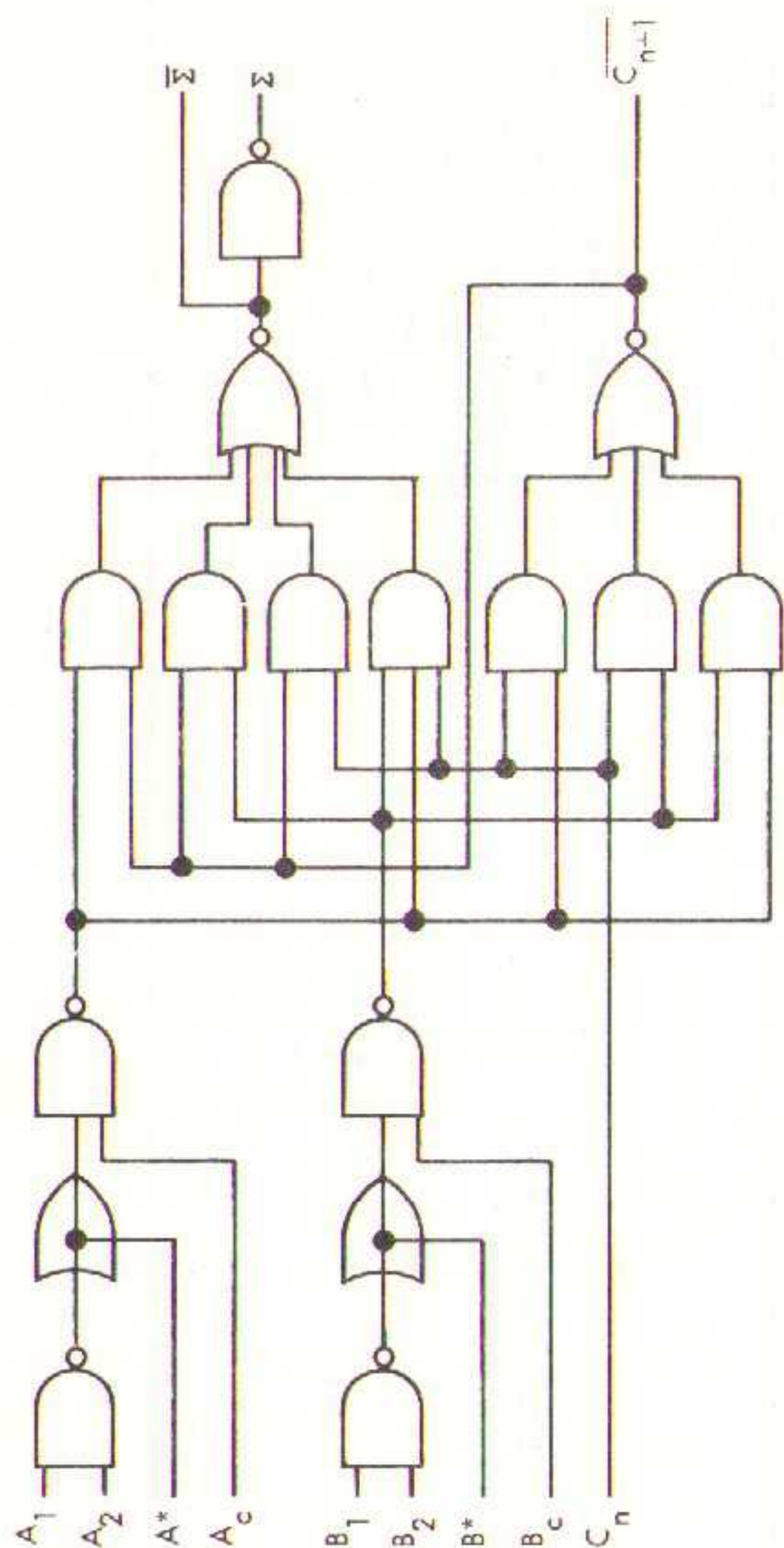
Operation is as follows: To add the contents of Register A1 to Register B1, A2 and B2 control lines are brought to the logical 0 state. In similar fashion, the contents of register A1 are added to register B2 by holding A2 and B1 control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A* and B* inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

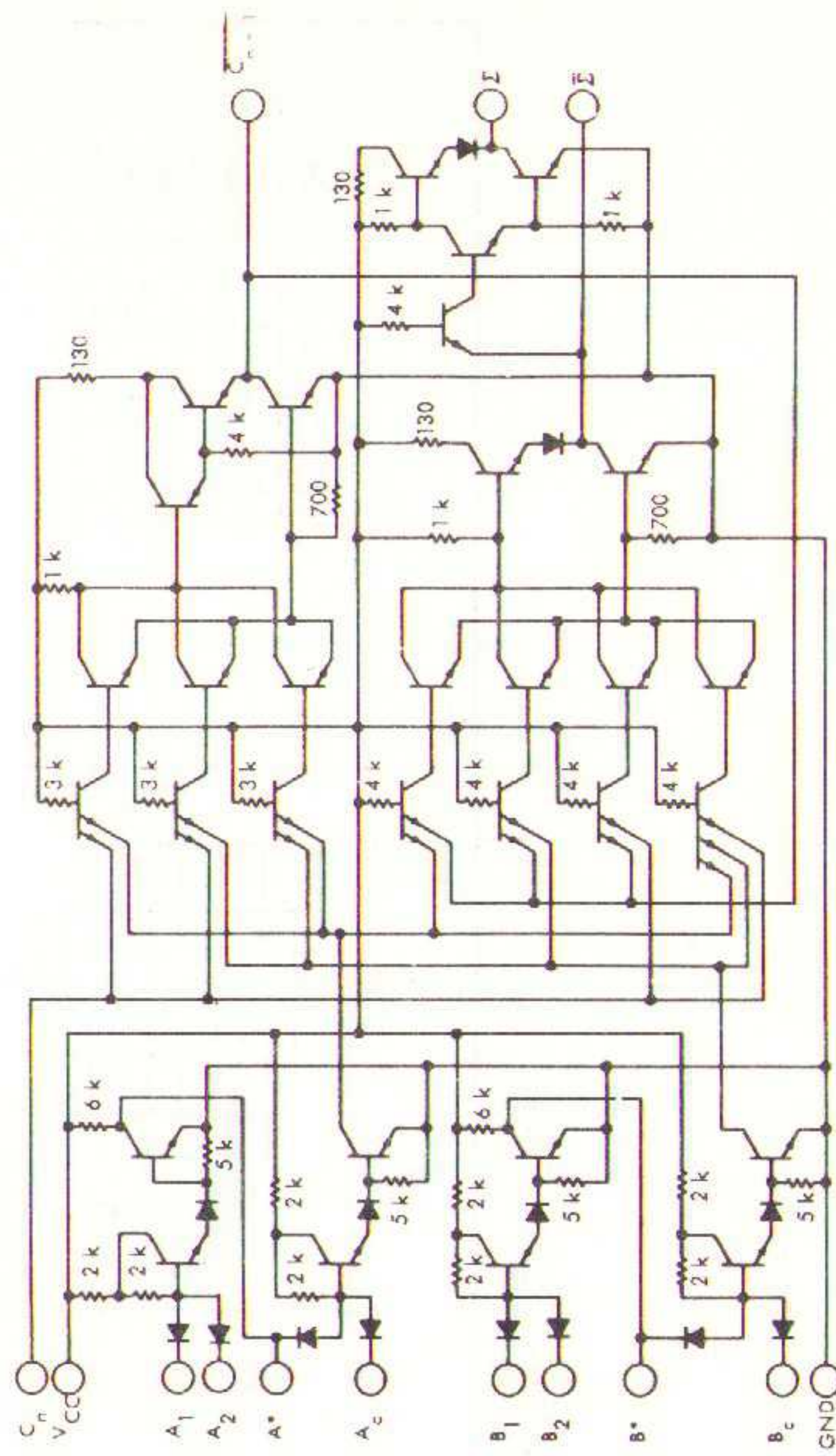
Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in Figure C. Inputs from the register-control gates (SN7405) of the additional registers would be Dot-OR'd connected with A2 and B2 registers at the A* and B* inputs.

To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.

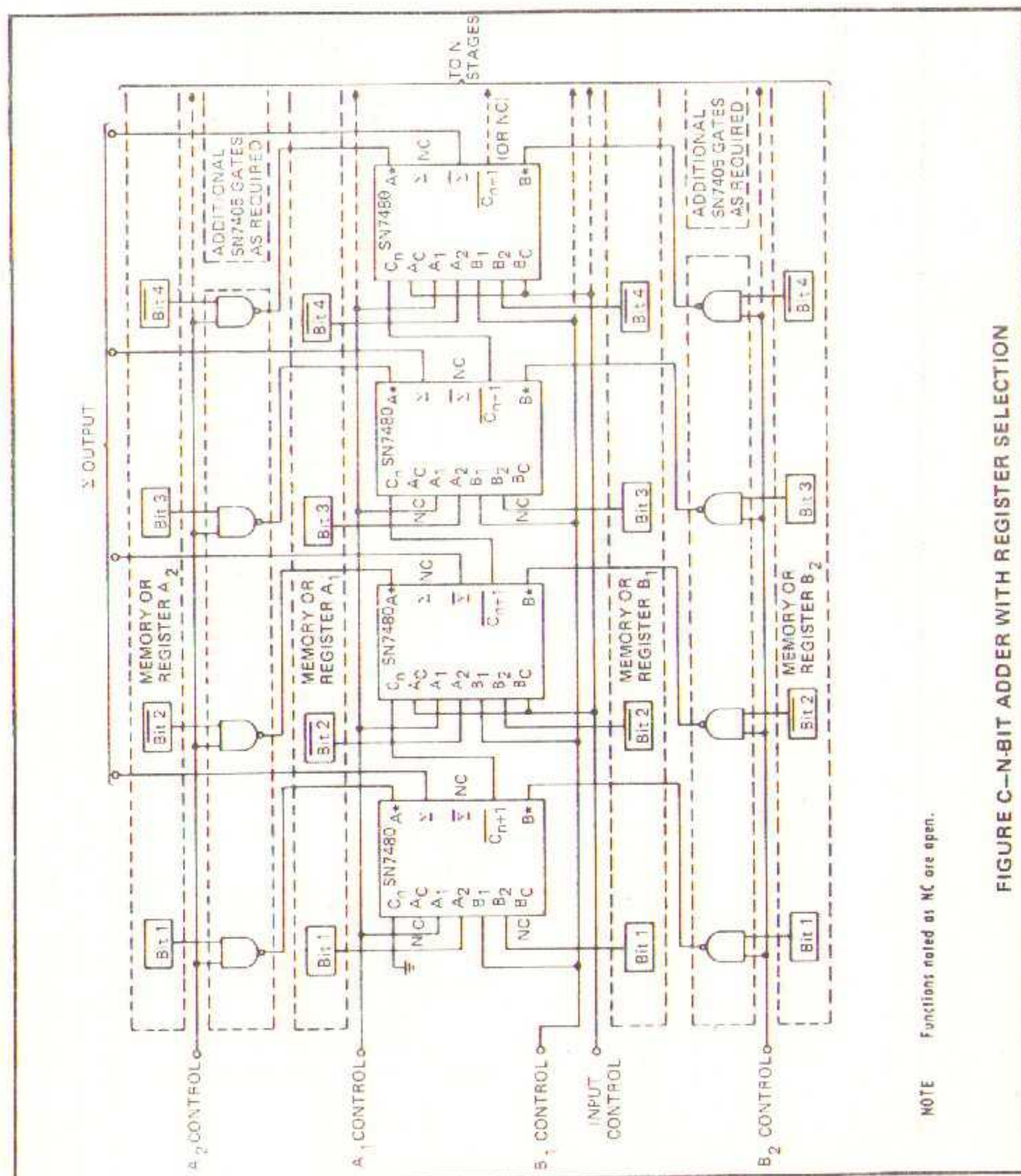
functional block diagram



schematic



Component values shown are nominal.
Resistor values are in ohms.

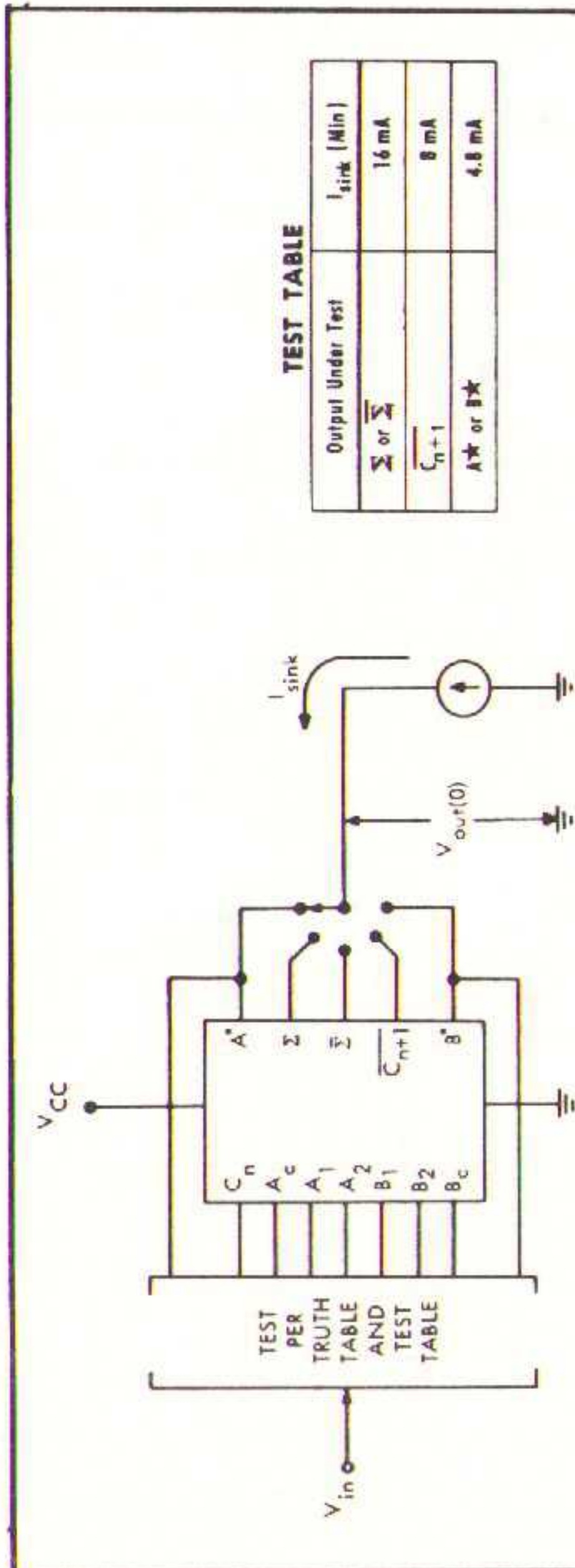


NOTE Functions noted at NC are open.

FIGURE C-N-BIT ADDER WITH REGISTER SELECTION

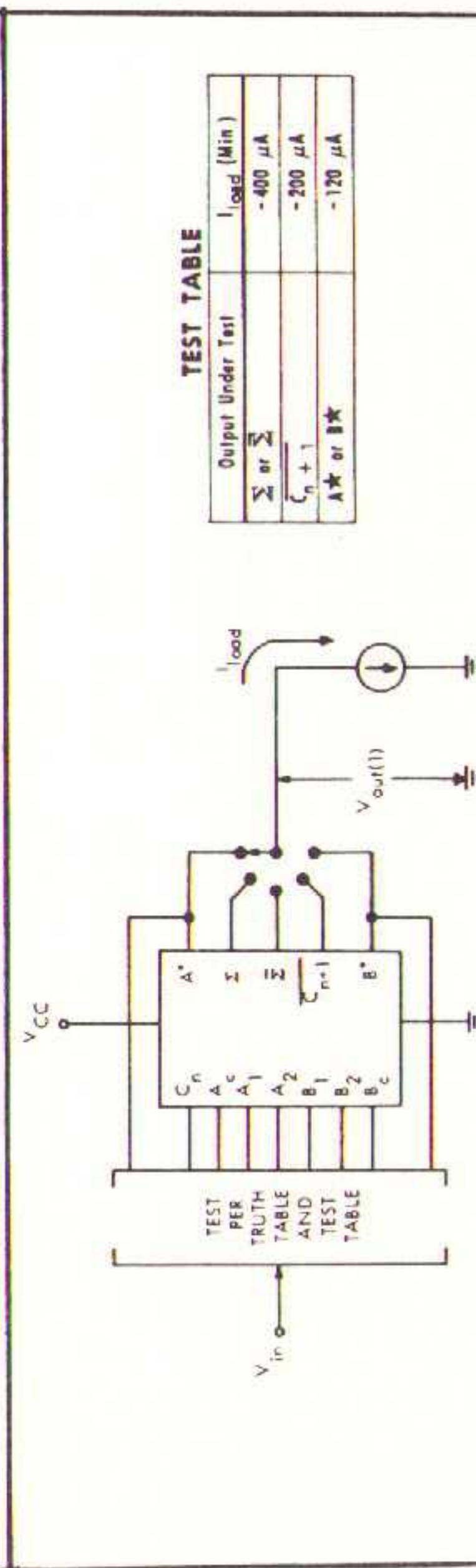
PARAMETER MEASUREMENT INFORMATION

d-c test circuits



1. Each input or output is tested separately.
2. When A^* is tested A_1 and A_2 are at GND. When B^* is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A^* or B^* respectively, is open.

FIGURE 1

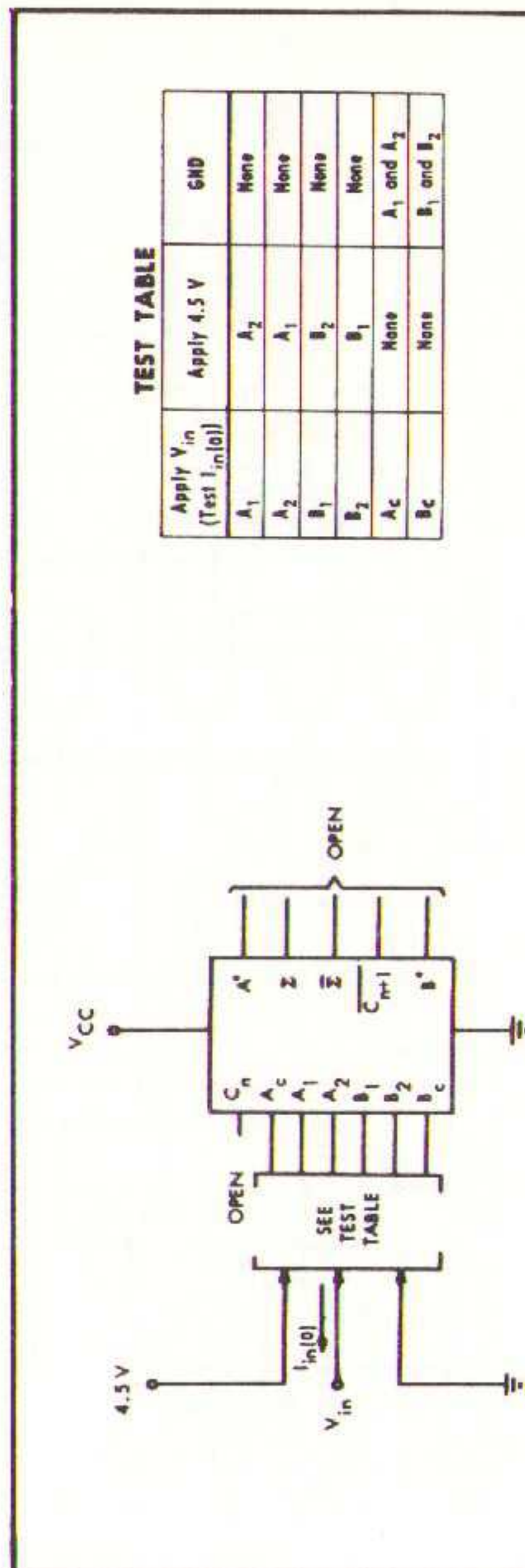


1. Each input or output is tested separately.
2. When A^* is tested A_1 and A_2 are at GND. When B^* is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A^* or B^* , respectively, is open.

FIGURE 2

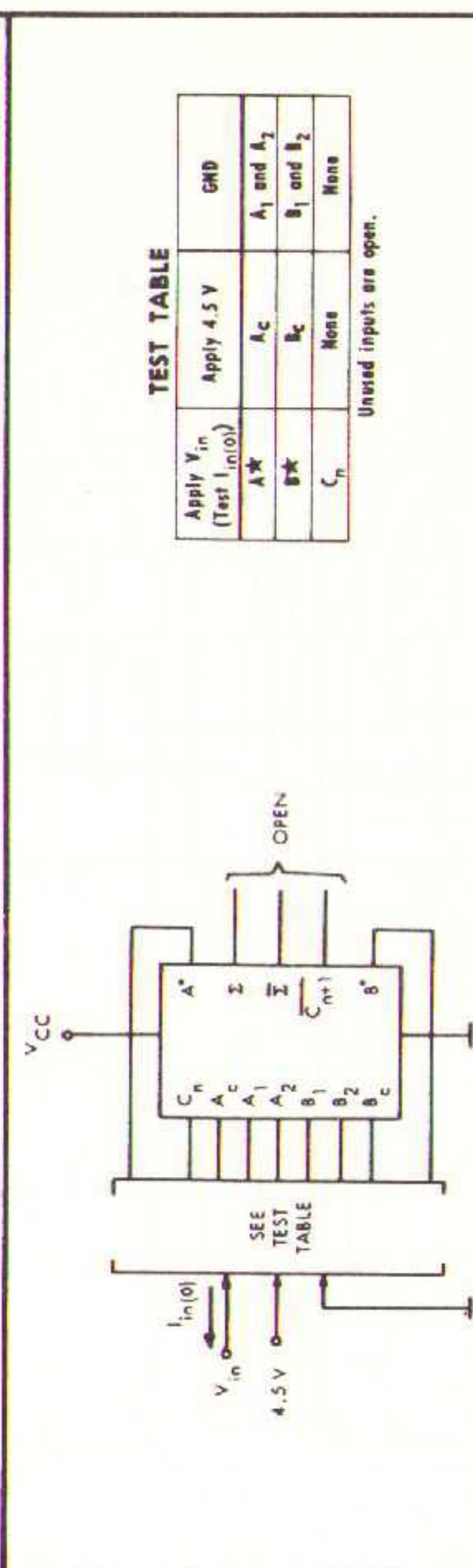
§Arrows indicate actual direction of current flow.

d-c test circuits (continued)



1. Each input is tested separately.

FIGURE 3



1. Each input is tested separately.

FIGURE 4

§Arrows indicate actual direction of current flow.

switching characteristics



1. Perform test in accordance with test table.

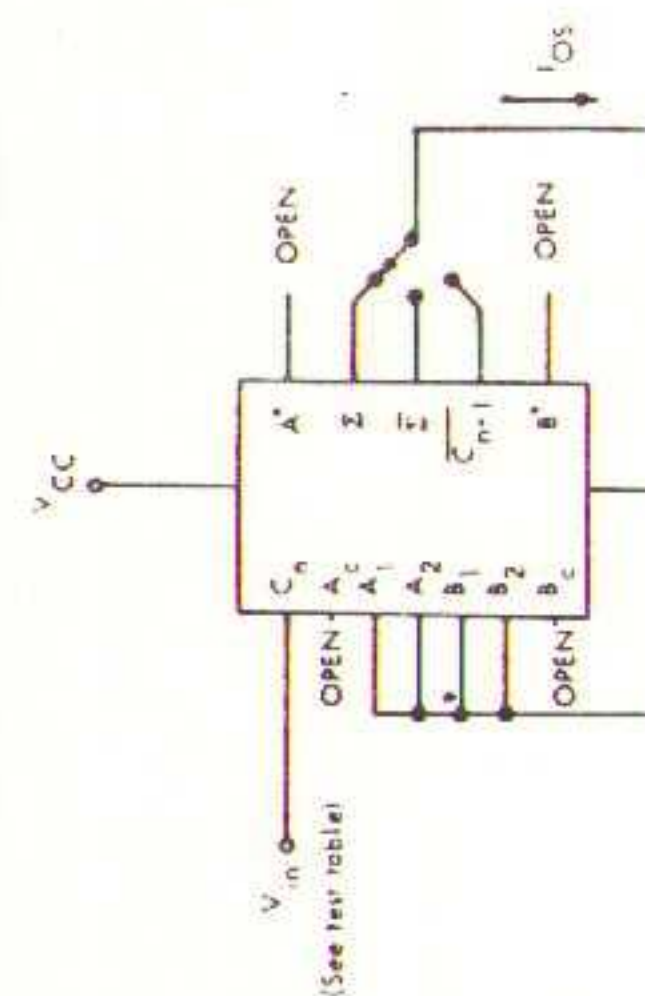
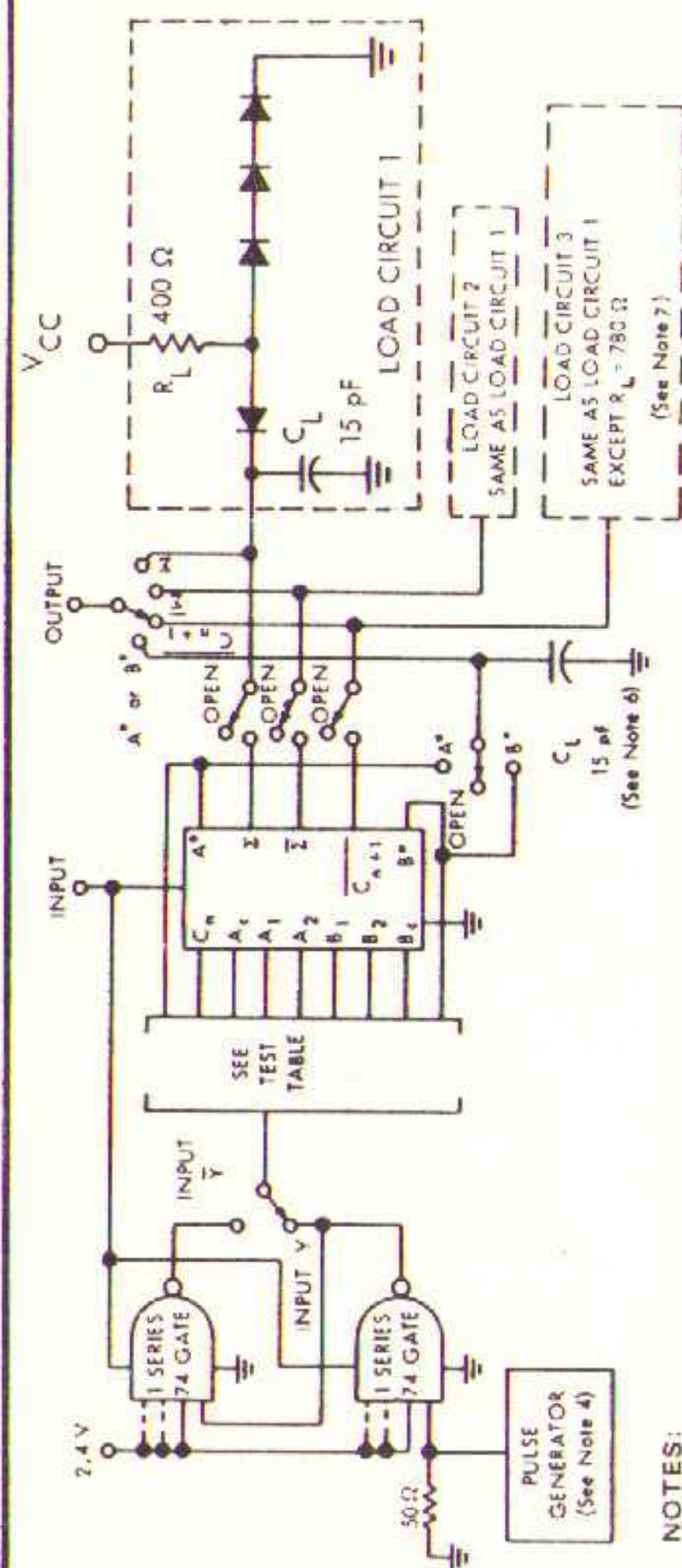


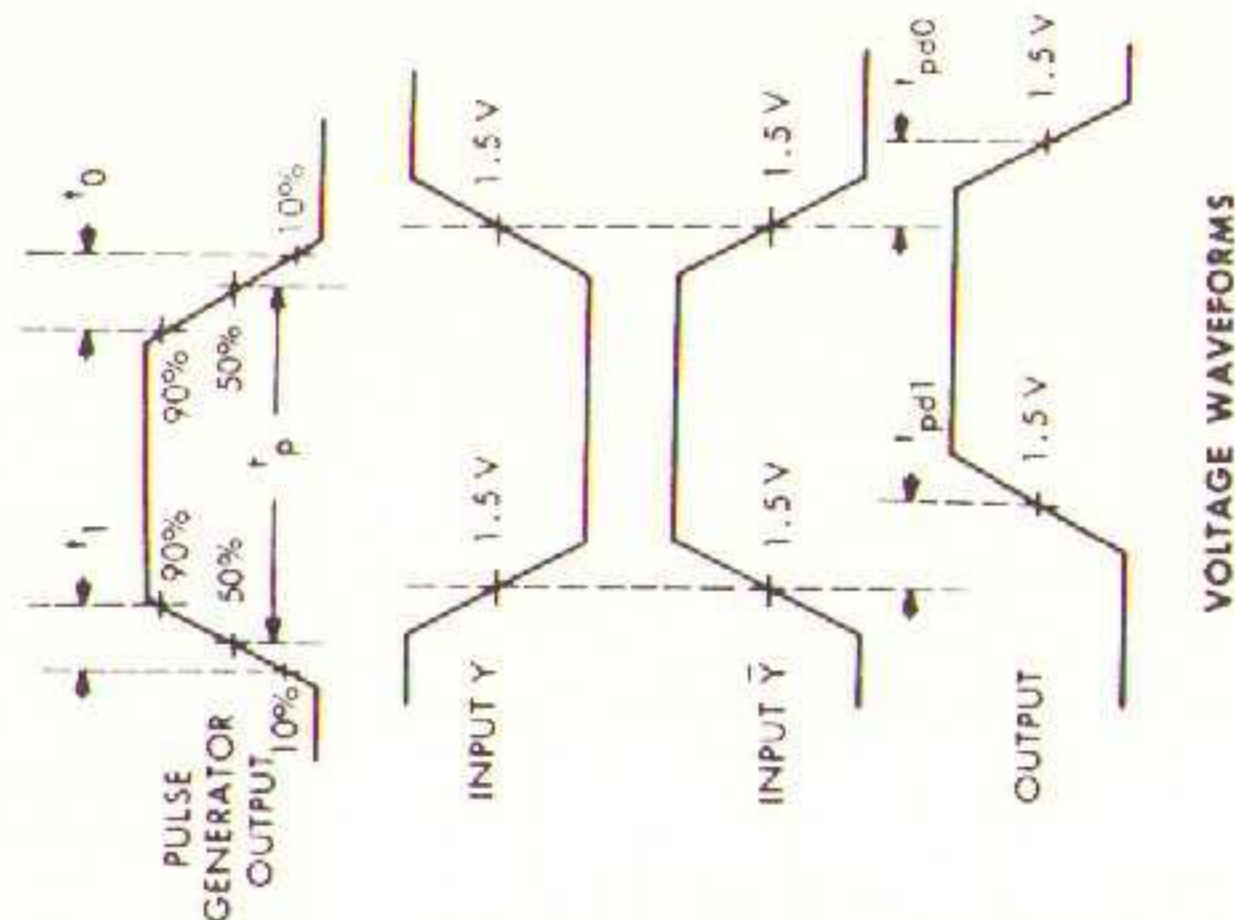
FIGURE 7

Arrows indicate actual direction of current flow.



- NOTES:**
1. Perform test in accordance with test table.
 2. Each output is tested separately.
 3. Voltage values are with respect to network GND terminal.
 4. The generator has the following characteristics: $V_{gen} = 3\text{ V}$, $t_1 = t_0 \leq 15\text{ ns}$, $t_p = 0.5\text{ }\mu\text{s}$, $PRR = 1\text{ MHz}$, and $Z_{out} \approx 50\text{ }\Omega$.
 5. Inputs and outputs not otherwise specified are open.
 6. C_L includes probe and jig capacitance.
 7. Load circuit 2 simulates output load of 5.
- All diodes are 1N3064.

TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE (See Note 5)

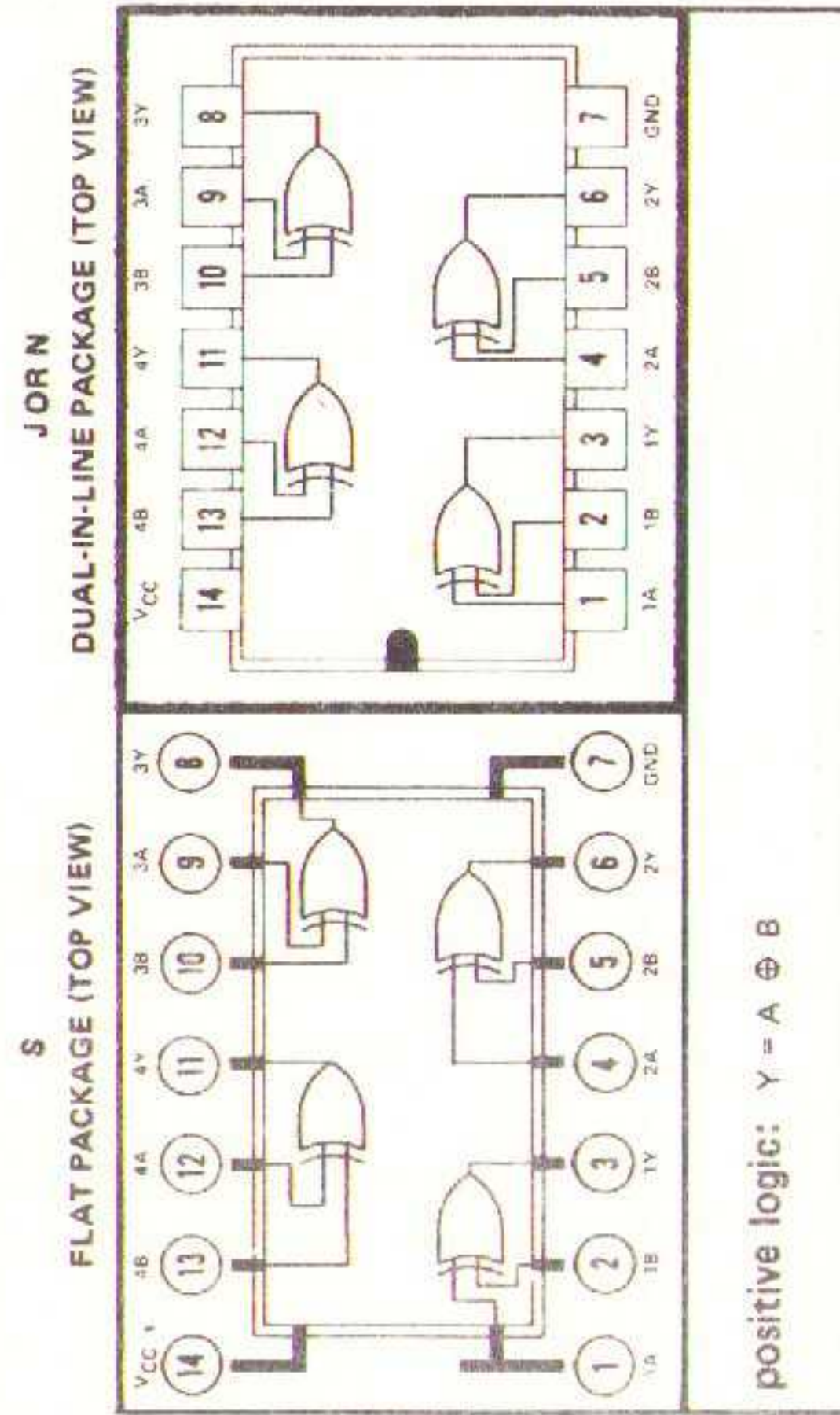
TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\bar{Y}$ TO	APPLY INPUT Y TO	APPLY + 2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_n + 1}$	None	C_n	None	B_1	$\overline{C_n + 1}$ ($N = 5$)
2	$C_n - 1$	None	C_n	None	B_1	$\overline{C_n + 1}$ ($N = 5$)
3	$\overline{C_n + 1}$	B_c	None	C_n	A_1, B_1	$\overline{C_n + 1}$ ($N = 5$)
4	$\overline{C_n + 1}$	B_c	None	C_n	A_1, B_1	$\overline{C_n + 1}$ ($N = 5$)
5	Σ	A_c	None	C_n	A_1, B_1	Σ ($N = 10$)
6	Σ	A_c	None	C_n	A_1, B_1	$\overline{C_n + 1}$ ($N = 5$)
7	Σ	B_c	None	C_n	B_1	Σ ($N = 10$)
8	Σ	B_c	None	C_n	B_1	Σ ($N = 10$)
9	$A \star$	None	A_1	A_1	None	$A \star$ ($C_L = 15 \text{ pF}$)
10	$A \star$	None	A_1	A_1	None	$A \star$ ($C_L = 15 \text{ pF}$)
11	$B \star$	None	B_1	B_1	None	$B \star$ ($C_L = 15 \text{ pF}$)
12	$B \star$	None	B_1	B_1	None	$B \star$ ($C_L = 15 \text{ pF}$)

FIGURE 9 – SWITCHING TIMES

- Input-Clamping Diodes Simplify System Design
- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Times: 12 ns

logic

TRUTH TABLE		
INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



description

Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\bar{B} + \bar{A}B$. When the input states are complementary, the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

The SN5486 is characterized for operation over the full military temperature range of -55°C to 125°C and the SN7486 is characterized for operation from 0°C to 70°C .

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Note 1)	5.5 V
Operating Case Temperature Range: SN5486S	-55°C to 125°C
Operating Free-Air Temperature Range: SN5486J, SN5486N	-55°C to 125°C
Storage Temperature Range: SN7486 Circuits	0°C to 70°C
NOTE 1: These voltage values are with respect to network ground terminal.	

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5486 Circuits	4.5	5	5.5	V
SN7486 Circuits	4.75	5	5.25	V
Normalized Fan-out from each output, N: Logical 0			10	
Logical 1			20	

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
$V_{in}(1)$ Input voltage required to ensure logical 1 at any input terminal	1	$V_{CC} = \text{MIN}$	2			V
$V_{in}(0)$ Input voltage required to ensure logical 0 at any input terminal	1	$V_{CC} = \text{MIN}$			0.8	V
$V_{out}(1)$ Logical 1 output voltage	1	$V_{CC} = \text{MIN}$, $V_{in}(1) = 2\text{ V}$, $V_{in}(0) = 0.8\text{ V}$, $I_{load} = -800\text{ }\mu\text{A}$	2.4			V
$V_{out}(0)$ Logical 0 output voltage	2	$V_{CC} = \text{MIN}$, $V_{in}(1) = 2\text{ V}$, $V_{in}(0) = 0.8\text{ V}$, $I_{sink} = 16\text{ mA}$			0.4	V
$I_{in}(1)$ Logical 1 level input current (each input)	3	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{ V}$			40	μA
		$V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{ V}$			1	mA
$I_{in}(0)$ Logical 0 level input current (each input)	4	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{ V}$			-1.6	mA
I_{OS} Short circuit output current §	5	$V_{CC} = \text{MAX}$, $V_{in}(1) = 4.5\text{ V}$, $V_{in}(0) = 0$	-20		-55	mA
		SN5486				
		SN7486			-55	mA
I_{CC} Supply current	6	$V_{CC} = \text{MAX}$, $V_{in} = 4.5\text{ V}$		30	43	mA
		SN5486		30	50	mA
		SN7486				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

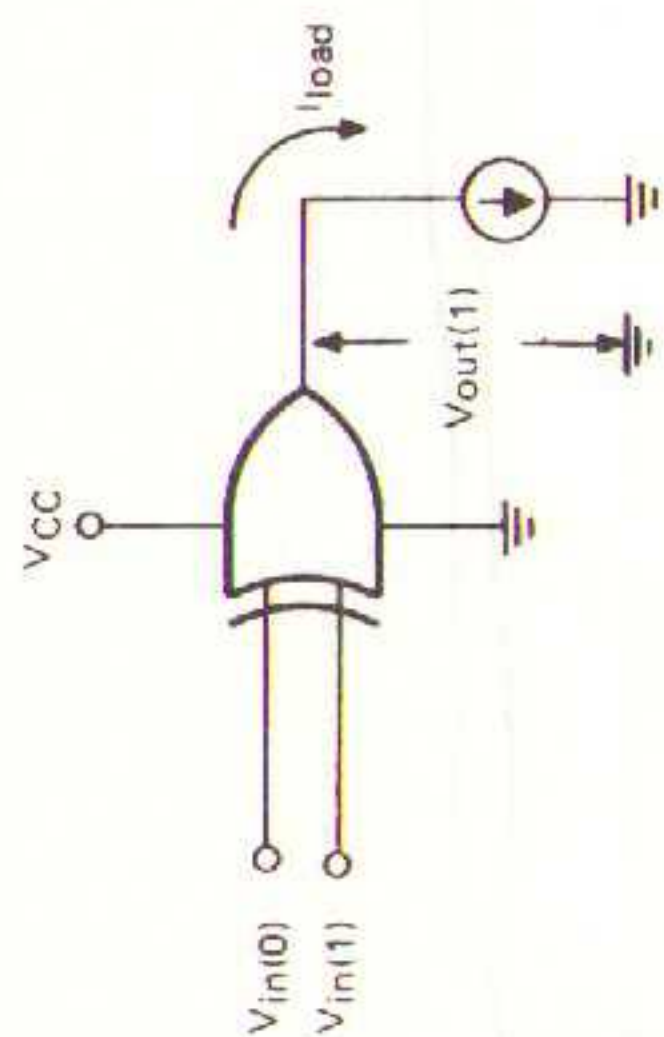
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level (other input low)	7	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		11	17	ns
t_{pd1} Propagation delay time to logical 1 level (other input low)	7	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		15	23	ns
t_{pd0} Propagation delay time to logical 0 level (other input high)	7	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		13	22	ns
t_{pd1} Propagation delay time to logical 1 level (other input high)	7	$C_L = 15\text{ pF}$, $R_L = 400\text{ }\Omega$		18	30	ns

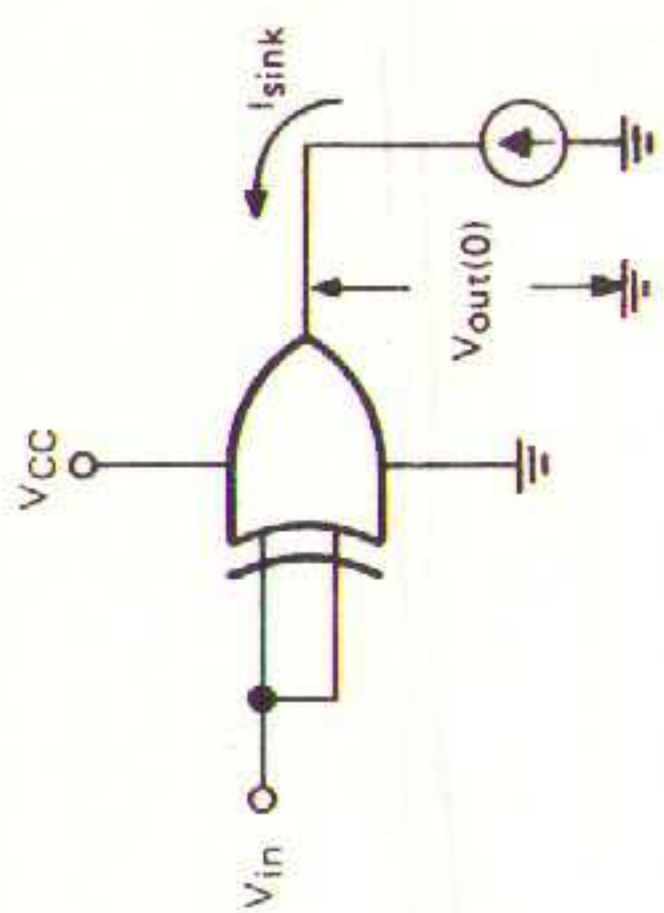
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



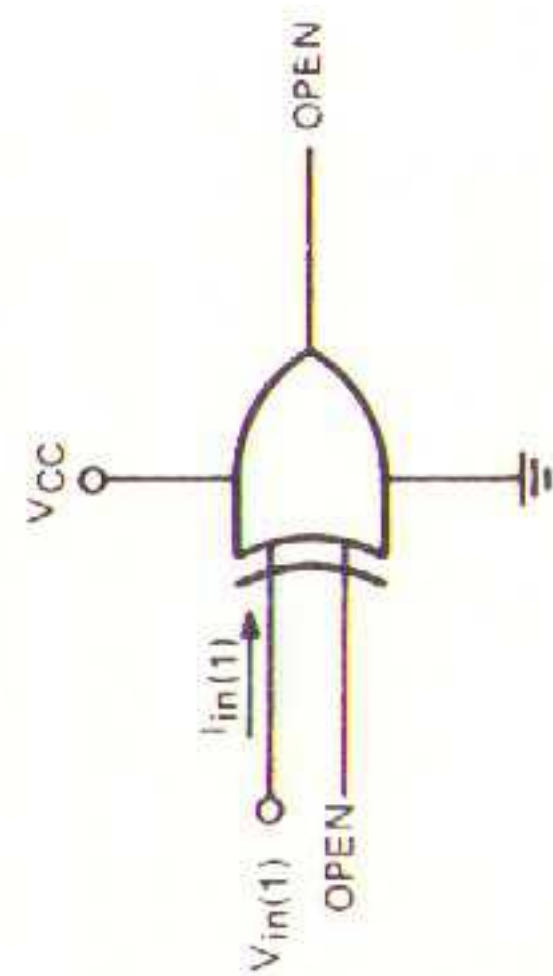
1. Each input is tested separately.

FIGURE 1



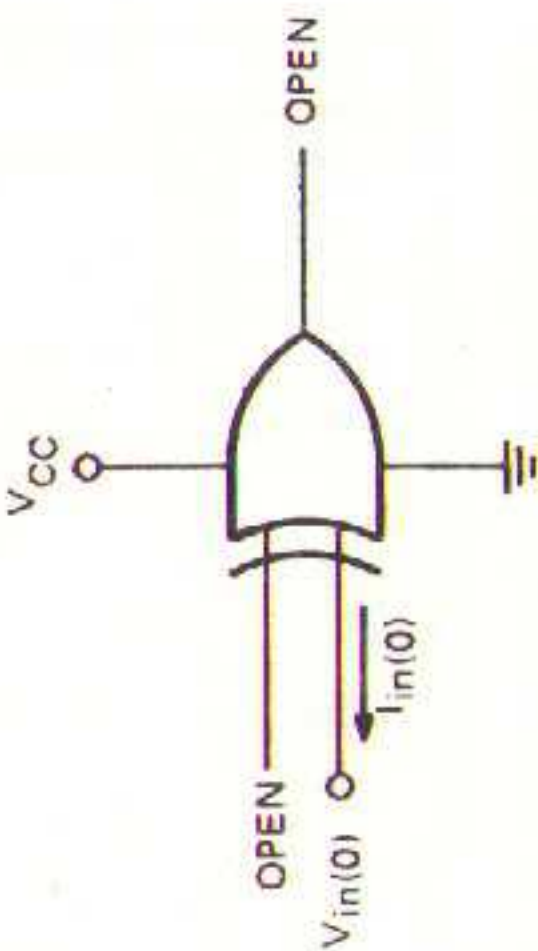
1. Logical 0 and logical 1 input conditions are tested.

FIGURE 2



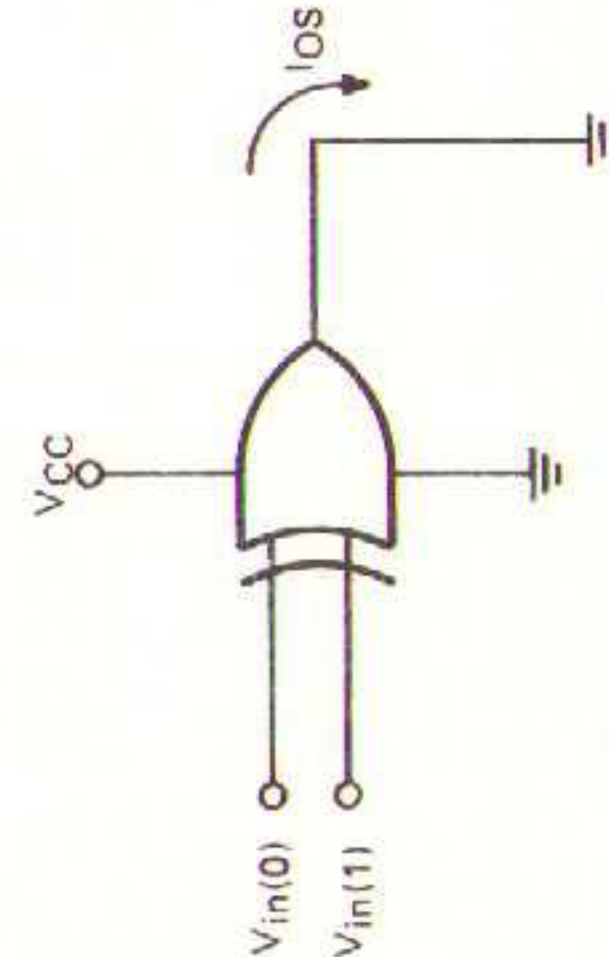
1. Each input is tested separately.

FIGURE 3



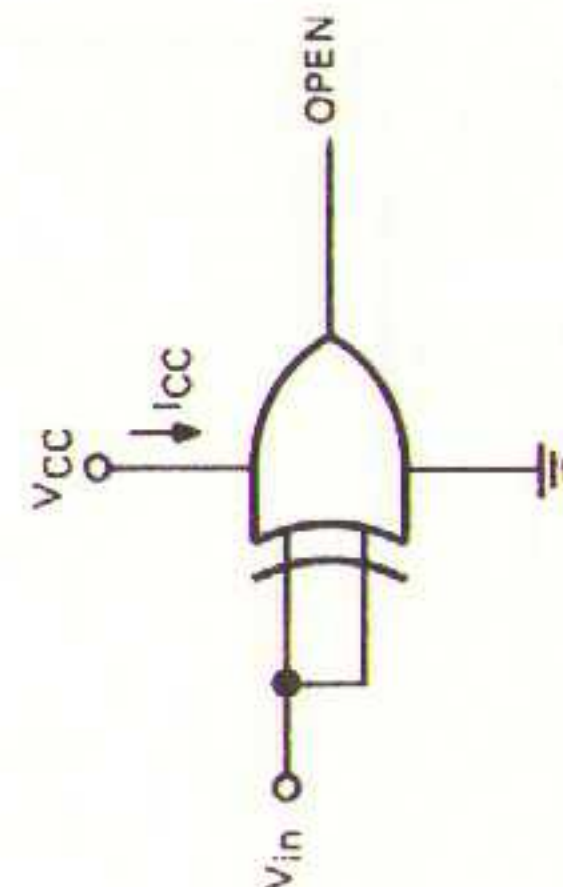
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5

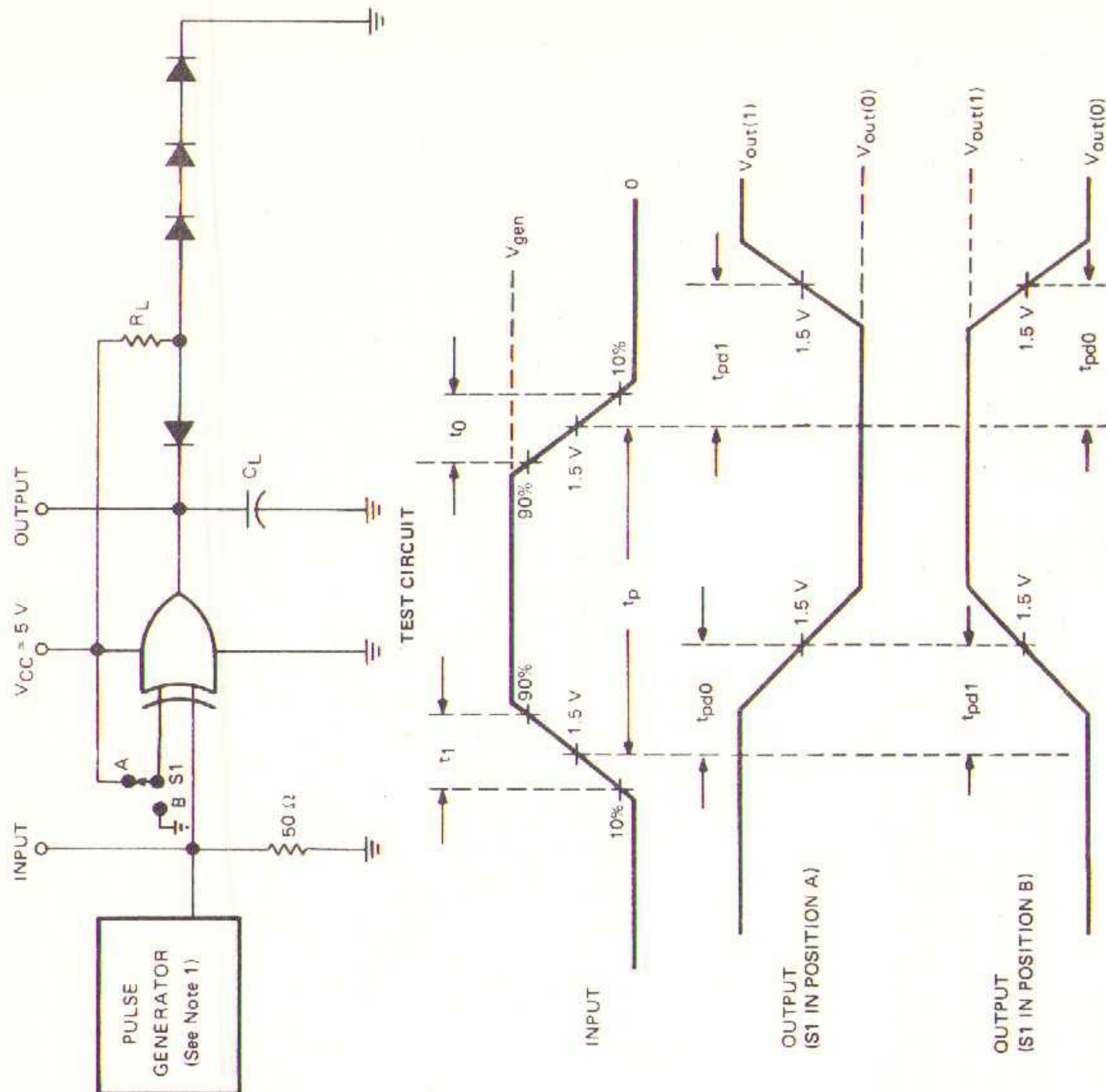


1. Each gate is tested separately.
2. Logical 0 and logical 1 input conditions are tested.

FIGURE 6

† Arrows indicate actual direction of current flow.

switching characteristics



VOLTAGE WAVEFORMS

- NOTES: 1. The generator has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 15\text{ ns}$, $t_p = 0.5\text{ }\mu\text{s}$, $PRR = 1\text{ MHz}$, $Z_{out} \approx 50\text{ }\Omega$.
2. All diodes are 1N3064.
3. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$.
4. C_L includes probe and jig capacitance.
5. Each gate tested separately.

FIGURE 7

MSI TTL HIGH-SPEED DECADE COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS	OUTPUT
R ₀ (1) R ₀ (2)	D C B A
1 1	0 0 0 0
1 1	0 0 0 1
1 1	0 0 1 0
1 1	0 0 1 1
1 1	0 1 0 0
1 1	0 1 0 1
1 1	0 1 1 0
1 1	0 1 1 1
1 1	1 0 0 0
1 1	1 0 0 1
1 1	1 0 1 0
1 1	1 0 1 1
1 1	1 1 0 0
1 1	1 1 0 1
1 1	1 1 1 0
1 1	1 1 1 1

NC—No Internal Connection

- NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

description and typical count configurations

These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to logical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

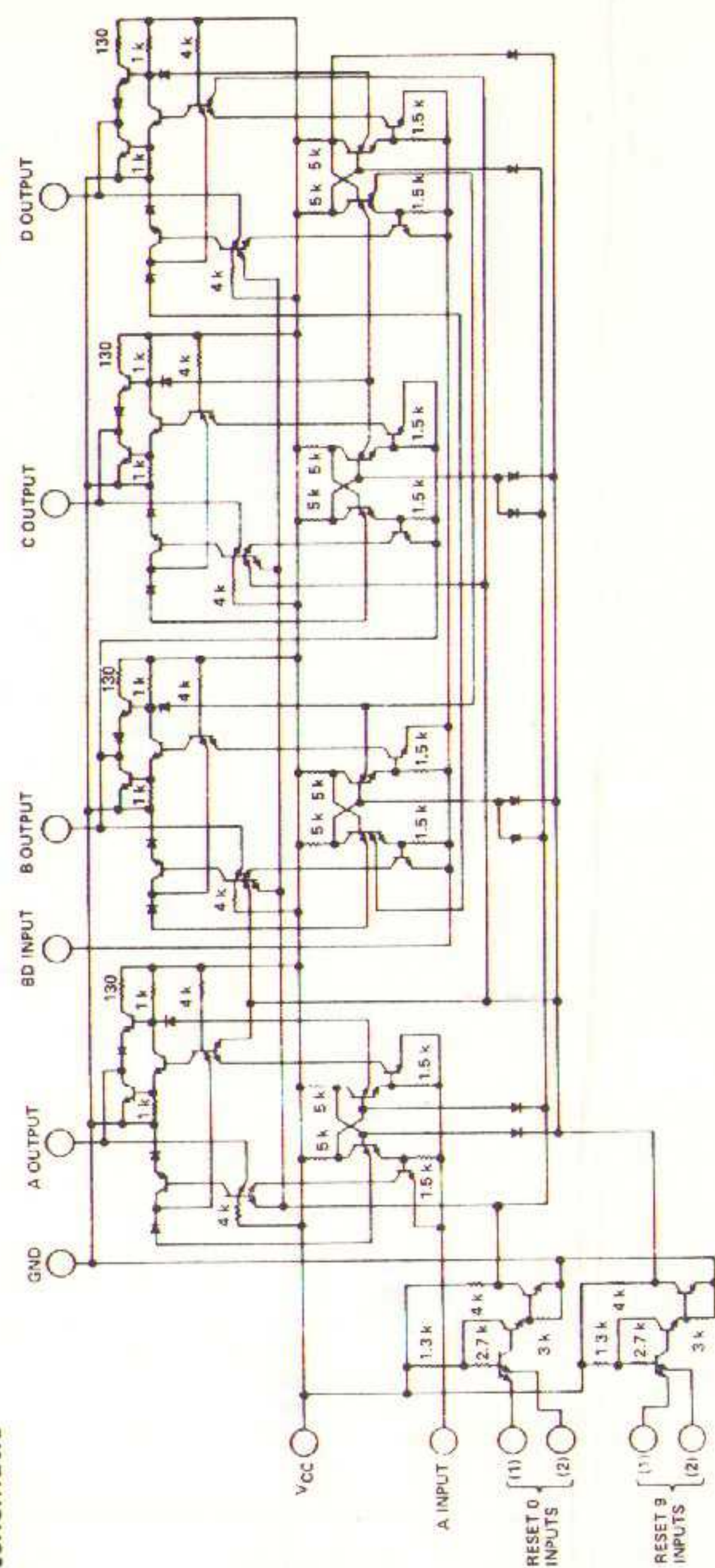
1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 160 mW.

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}		Maximum frequency of input count pulses $C_L = 15 pF$, $R_L = 400 \Omega$	10	18		MHz
t_{pd1}	6	Propagation delay time to logical 1 level from input count pulse to output C $C_L = 15 pF$, $R_L = 400 \Omega$		60	100	ns
t_{pd0}	6	Propagation delay time to logical 0 level from input count pulse to output C $C_L = 15 pF$, $R_L = 400 \Omega$		60	100	ns

schematic



Component values shown are nominal.
Resistor values are in ohms.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3)	7 V
Input Voltage V_{in} (See Notes 3 and 4)	5.5 V
Operating Case Temperature Range: SN5490S	-55°C to 125°C
Operating Free-Air Temperature Range: SN5490J, SN5490N	-55°C to 125°C
SN7490 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5490 Circuits	4.5	5	5.5	V
SN7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 5)	50		10	
Width of Input Count Pulse, $t_p(in)$	50			ns
Width of Reset Pulse, $t_p(reset)$	50			ns

NOTE 5. Fan-out from output A to input BD and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	1	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	2	$V_{CC} = \text{MIN}$		0.8		V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = \text{MIN}, I_{load} = -400 \mu A$	2.4			V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = \text{MIN}, I_{sink} = 16 \text{ mA}$		0.4		V
Logical 1 level input current at $R_0(1), R_0(2), R_g(1),$ or $R_g(2)$	3	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$		40		μA
		$V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$		1		mA
Logical 1 level input current at input A	3	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$		80		μA
		$V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$		1		mA
Logical 1 level input current at input BD	3	$V_{CC} = \text{MAX}, V_{in} = 2.4 \text{ V}$		160		μA
		$V_{CC} = \text{MAX}, V_{in} = 5.5 \text{ V}$		1		mA
Logical 0 level input current at $R_0(1), R_0(2), R_g(1),$ or $R_g(2)$	4	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-1.6		mA
Logical 0 level input current at input A	4	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-3.2		mA
Logical 0 level input current at input BD	4	$V_{CC} = \text{MAX}, V_{in} = 0.4 \text{ V}$		-6.4		mA
Short-circuit output current§	5	$V_{CC} = \text{MAX}, V_{out} = 0 \text{ V}$	-20		-57	mA
			-18		-57	mA
Supply current	3	$V_{CC} = \text{MAX}, V_{in} = 4.5 \text{ V}$		32	46	mA
				32	53	mA

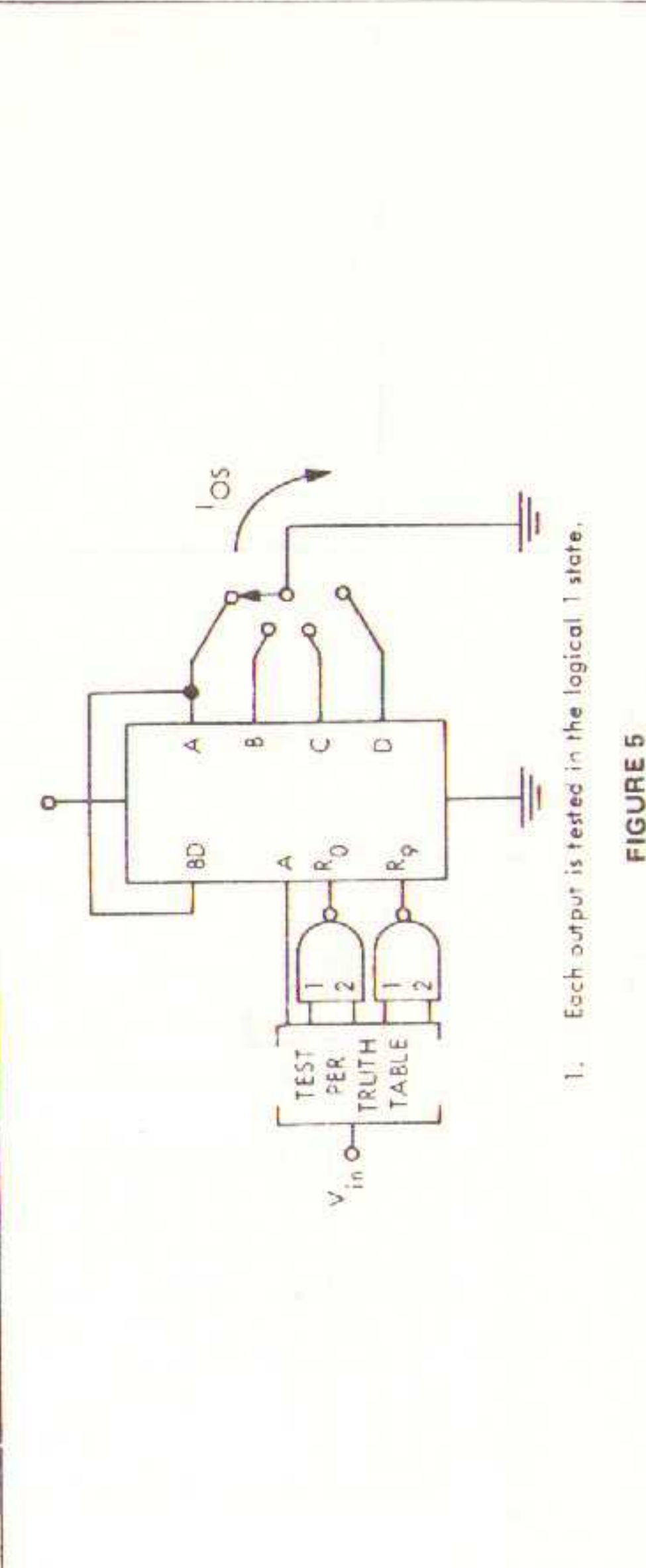
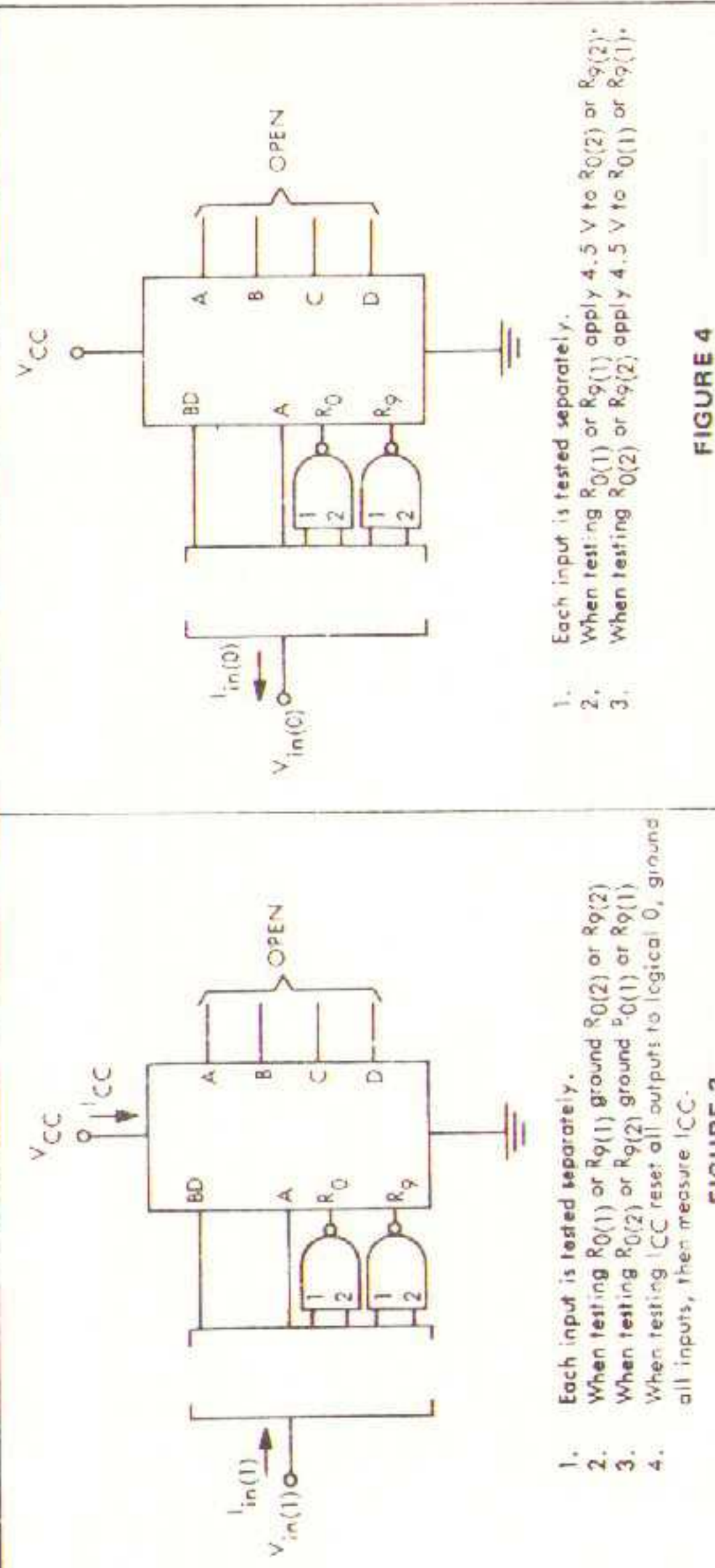
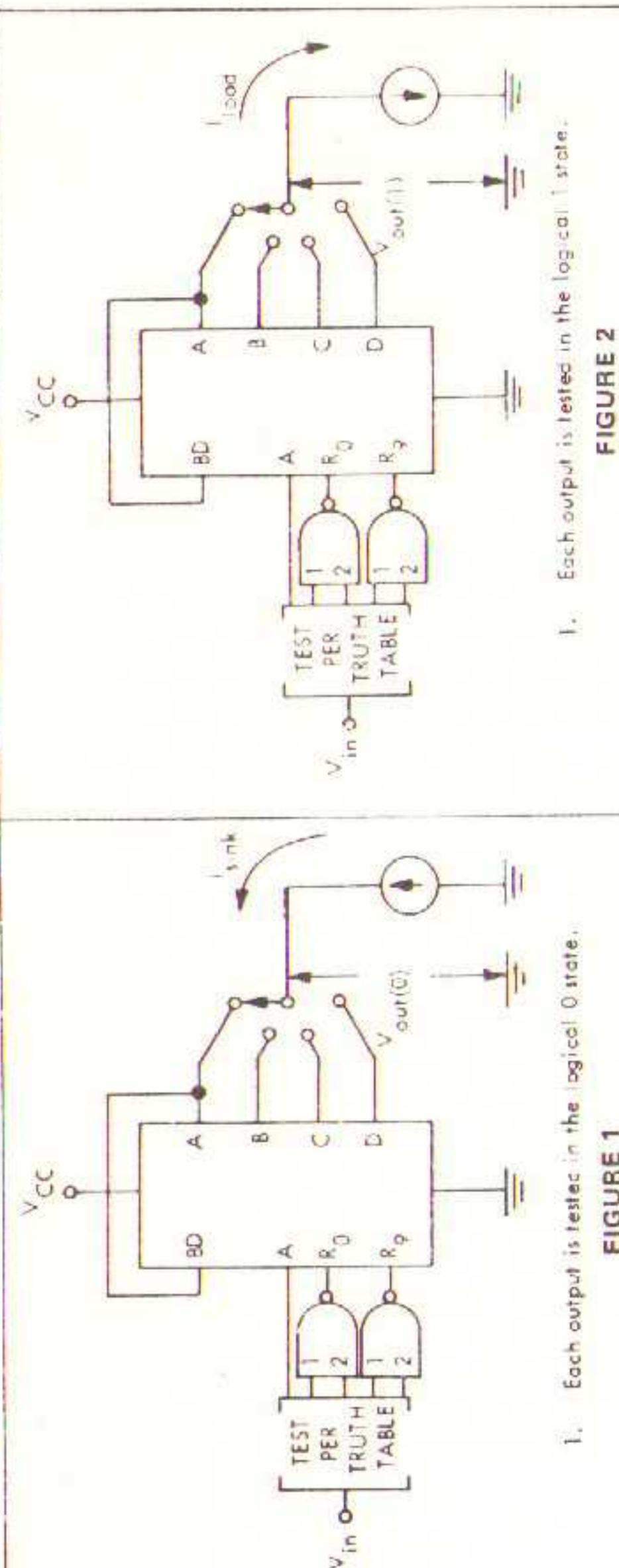
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

PARAMETER MEASUREMENT INFORMATION

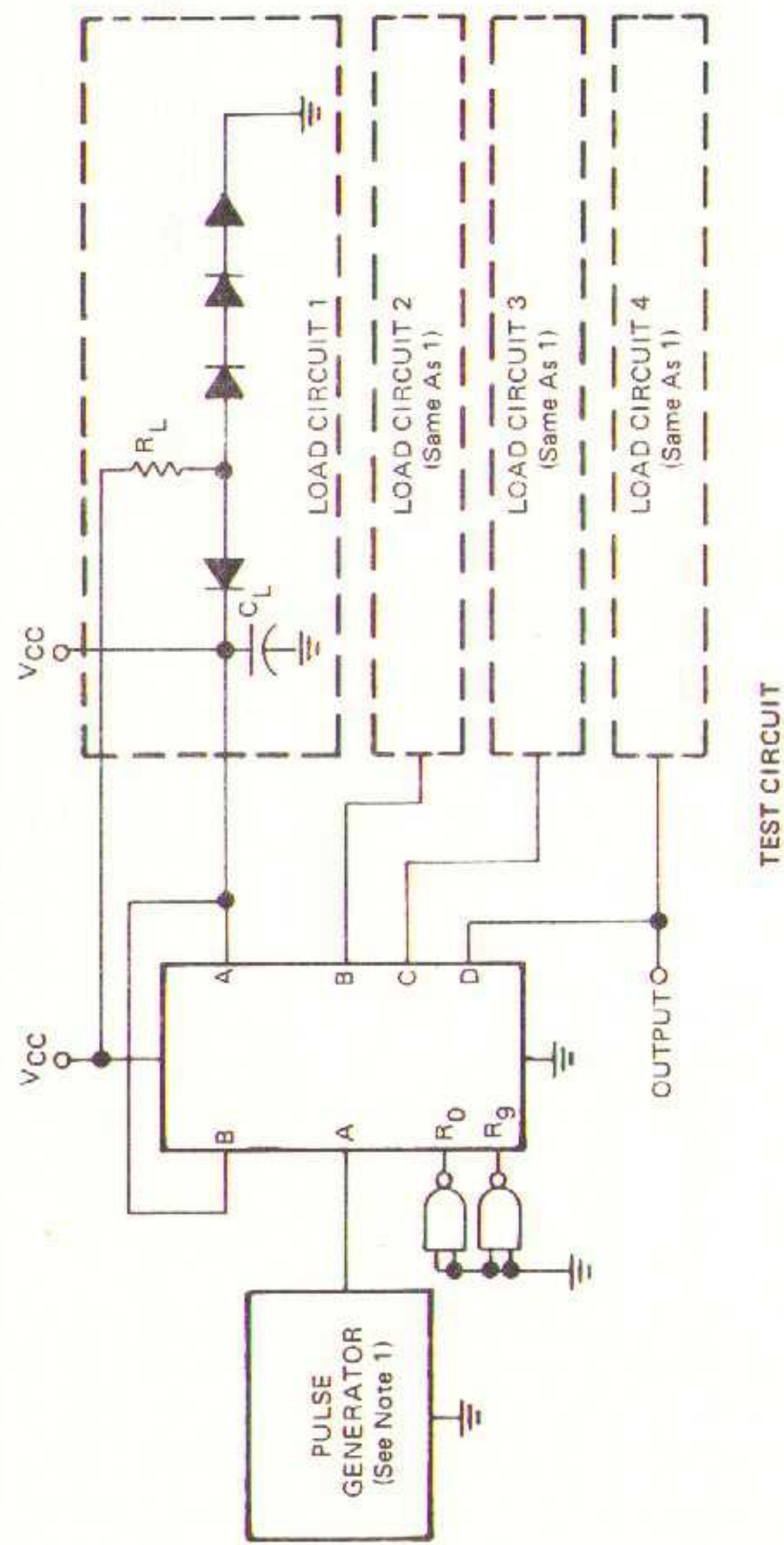
d-c test circuits†



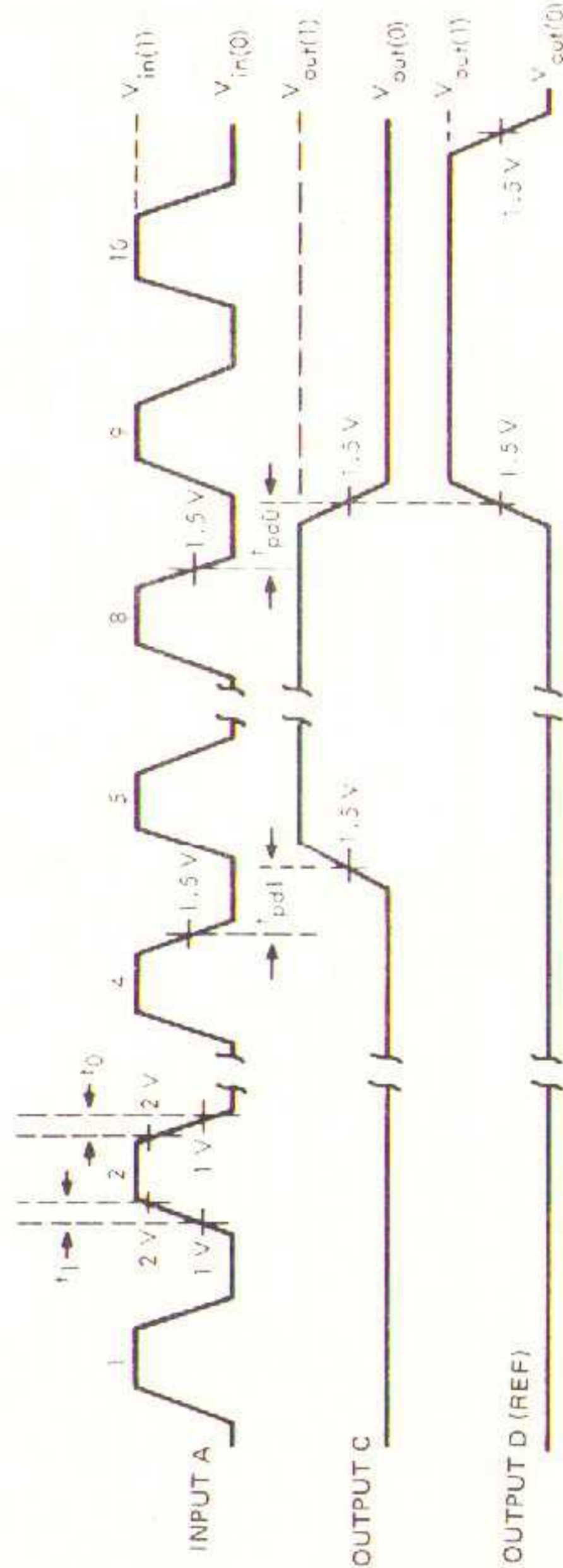
† Arrows indicate actual direction of current flow.

switching characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: 1. The pulse generator has the following characteristics: $V_{gen} = 3\text{ V}$, $t_0 = t_1 \leq 15\text{ ns}$, $t_p = 0.5\text{ }\mu\text{s}$, $P_{RR} = 1\text{ MHz}$, $Z_{out} \approx 50\text{ }\Omega$.
 2. All diodes are 1N3064.
 3. C_L includes probe and jig capacitance.
 4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
 5. Voltage values are with respect to ground terminal.

FIGURE 6 - SWITCHING TIMES

MSI TTL HIGH-SPEED COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

- NOTES: 1. Output A connected to input B.
 2. To reset all outputs to logical 0 both $R_0(1)$ and $R_0(2)$ inputs must be at logical 1.
 3. Either (or both) reset inputs $R_0(1)$ and $R_0(2)$ must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table above.
2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency divisions of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 155 mW.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4)	7 V
Input Voltage V_{in} (See Notes 4 and 5)	5.5 V
Operating Case Temperature Range	-55°C to 125°C
Operating Free-Air Temperature Range	-55°C to 125°C
Storage Temperature Range	0°C to 70°C

- NOTES: 4. These voltage values are with respect to network ground terminal.
 5. Input signals must be zero or positive with respect to network ground terminal.

schematic

Supply Voltage VCC (See Note 4): SN5492 Circuits
SN7492 Circuits

Normalized Fan-Out From Each Output (See Note 6)

Width of Input Count Pulse, t_p (in)

Width of Reset Pulse, t_{res} (in)

NOTE: a Fan-out from output A to input BC and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

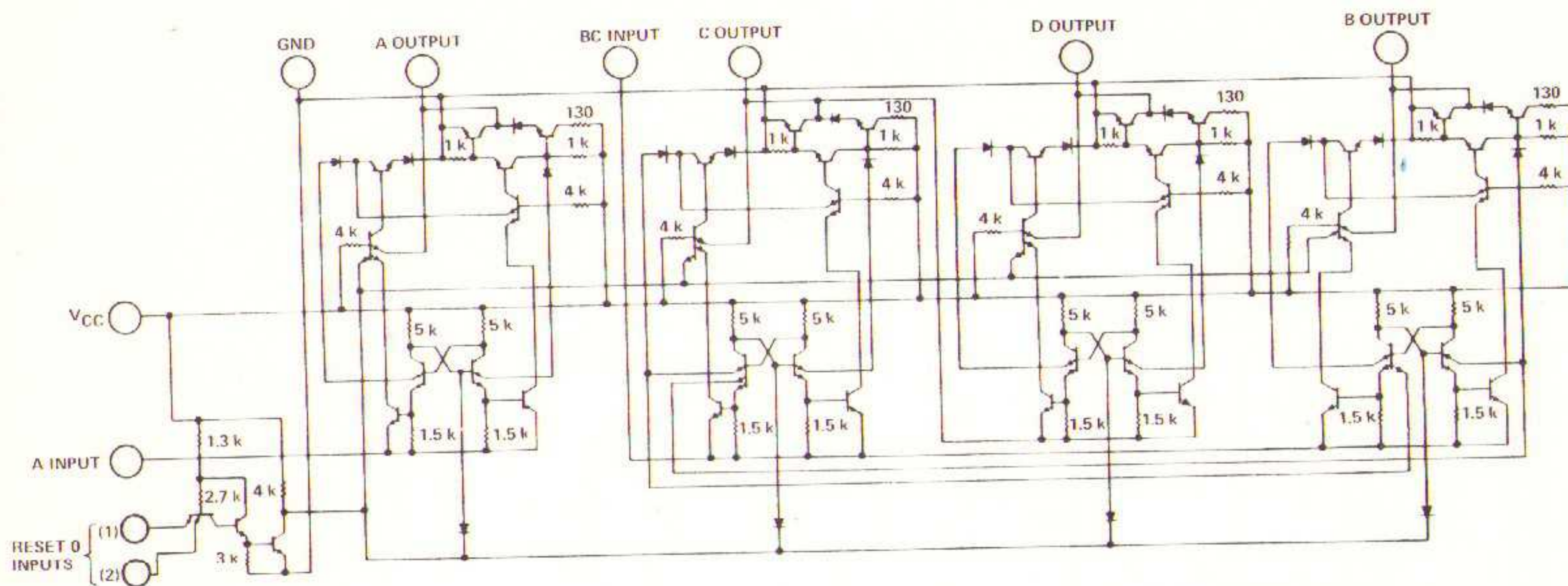
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$		$C_L = 15 \text{ pF}, R_L = 400 \Omega$	10	18		MHz
t_{pd1}	6	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		60	100	ns
t_{pd0}	6	$C_L = 15 \text{ pF}, R_L = 400 \Omega$		60	100	ns



Component values shown are nominal
Resistor values are in ohms.

MSI TTL HIGH-SPEED RIPPLE-THROUGH COUNTERS

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	INPUT				OUTPUT			
	A	B	C	D	Q	Q	Q	Q
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
10	1	0	1	0	1	0	1	0
11	1	0	1	1	1	0	1	1
12	1	1	0	0	1	1	0	0
13	1	1	0	1	1	1	0	1
14	1	1	1	0	1	1	1	0
15	1	1	1	1	1	1	1	1

- NOTES: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both RQ(1) and RQ(2) inputs must be at logical 1.
3. Either (or both) reset inputs RQ(1) and RQ(2) must be at a logical 0 to count.

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 32 mW per flip-flop (128 mW total).

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage VCC (See Note 4)	7 V
Input Voltage, V _{in} (See Notes 4 and 5)	5.5 V
Operating Case Temperature Range	-55°C to 125°C
Operating Free-Air Temperature Range	-55°C to 125°C
	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

- NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage VCC (See Note 4): SN5493 Circuits	4.5	5	5.5	V
SN7493 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, t _p (in)	50			ns
Width of Reset Pulse, t _p (reset)	50			ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

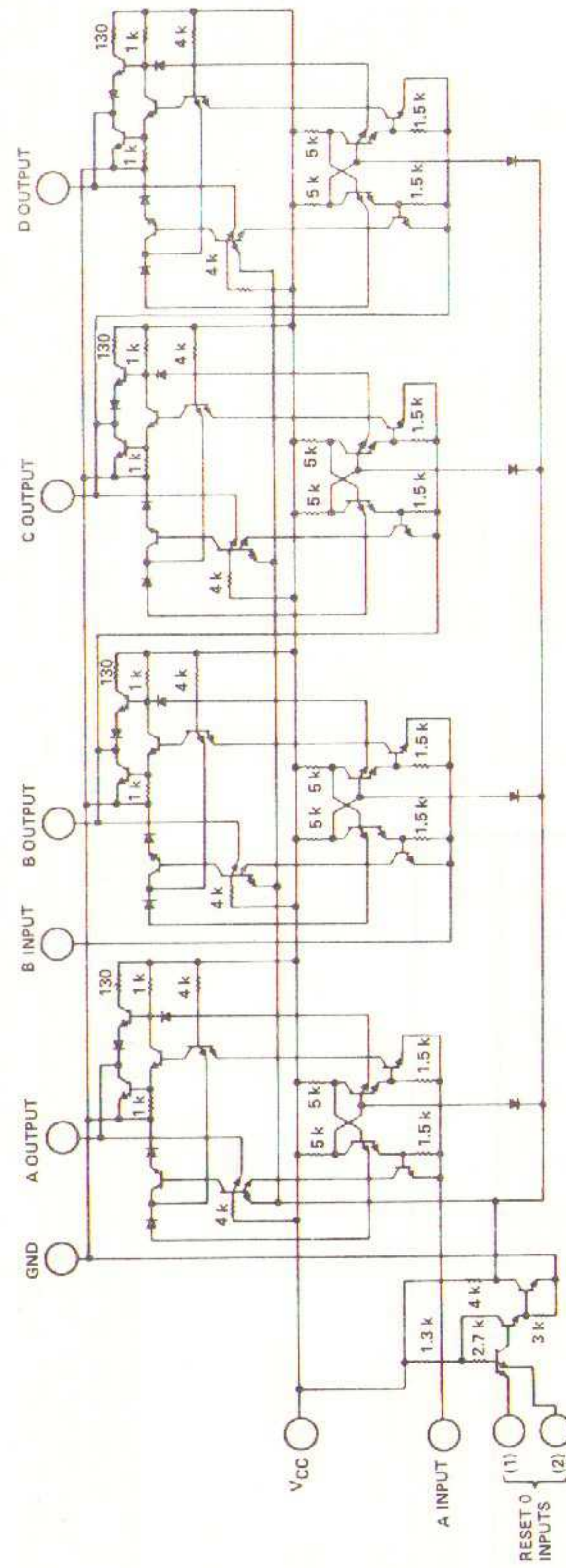
PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{in} (1) Input voltage required to ensure logical 1 at any input terminal	1	V _{CC} = MIN	2			V
V _{in} (0) Input voltage required to ensure logical 0 at any input terminal	2	V _{CC} = MIN			0.8	V
V _{out} (1) Logical 1 output voltage	2	V _{CC} = MIN, I _{load} = -400 μA	2.4			V
V _{out} (0) Logical 0 output voltage	1	V _{CC} = MIN, I _{sink} = 16 mA			0.4	V
I _{in} (1) Logical 1 level input current at RQ(1) or RQ(2) inputs	3	V _{CC} = MAX, V _{in} = 2.4 V			40	μA
		V _{CC} = MAX, V _{in} = 5.5 V			1	mA
I _{in} (1) Logical 1 level input current at A or B inputs	3	V _{CC} = MAX, V _{in} = 2.4 V			80	μA
		V _{CC} = MAX, V _{in} = 5.5 V			1	mA
I _{in} (0) Logical 0 level input current at RQ(1) or RQ(2) inputs	4	V _{CC} = MAX, V _{in} = 0.4 V			-1.6	mA
I _{in} (0) Logical 0 level input current at A or B inputs	4	V _{CC} = MAX, V _{in} = 0.4 V			-3.2	mA
I _{OS} Short-circuit output current§	5	V _{CC} = MAX, V _{out} = 0	-20		-57	mA
		V _{CC} = MAX, V _{in} = 4.5 V	-18		-57	mA
I _{CC} Supply current	3	V _{CC} = MAX, V _{in} = 4.5 V	32		46	mA
			32		53	mA

- † For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max} Maximum frequency of input count pulses		C _L = 15 pF, R _L = 400 Ω	10	18		MHz
t _{pd1} Propagation delay time to logical 1 level from input count pulse to output D	6	C _L = 15 pF, R _L = 400 Ω		75	135	ns
t _{pd0} Propagation delay time to logical 0 level from input count pulse to output D	6	C _L = 15 pF, R _L = 400 Ω		75	135	ns

schematic



Component values shown are nominal.
Resistor values are in ohms.

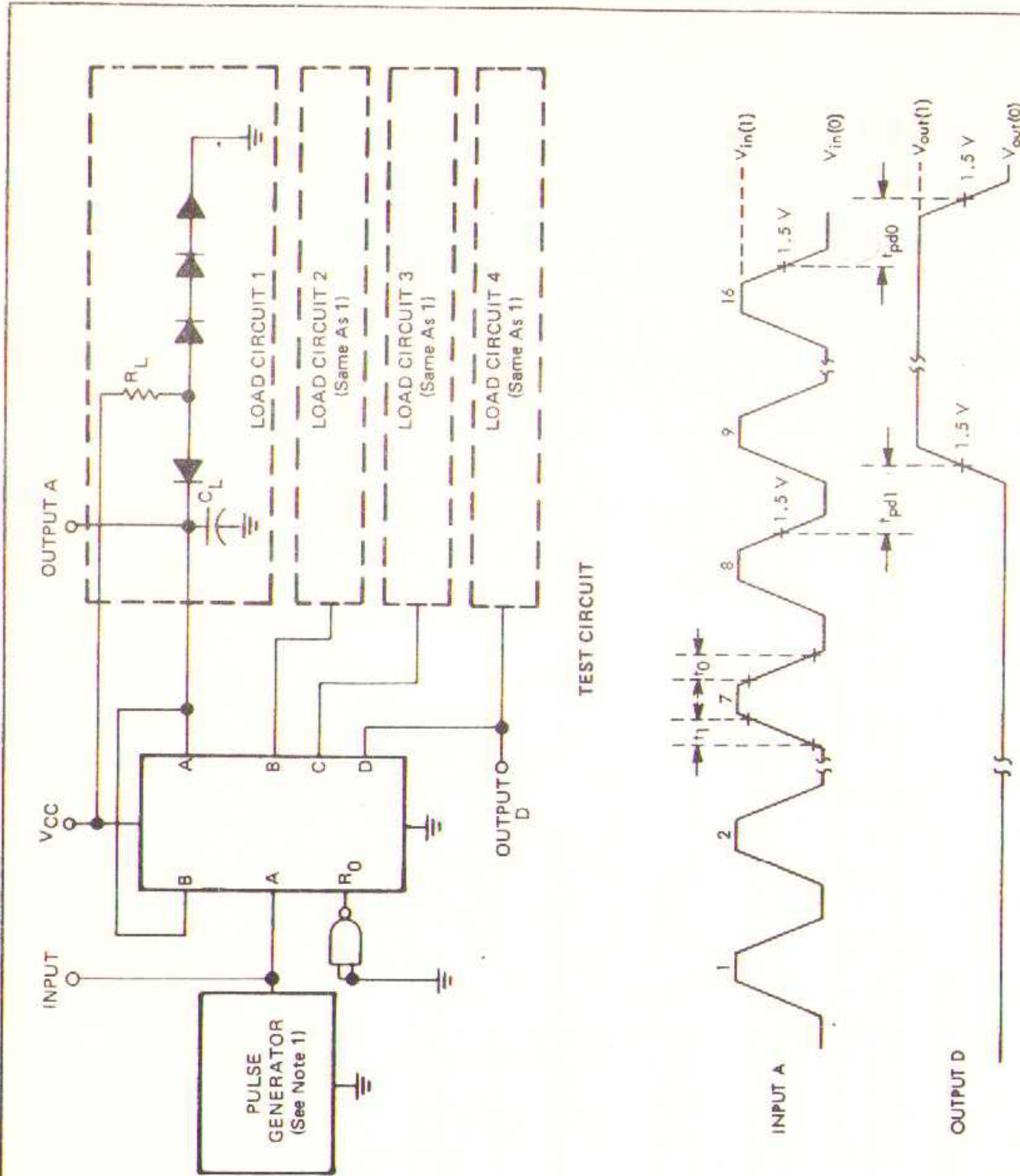
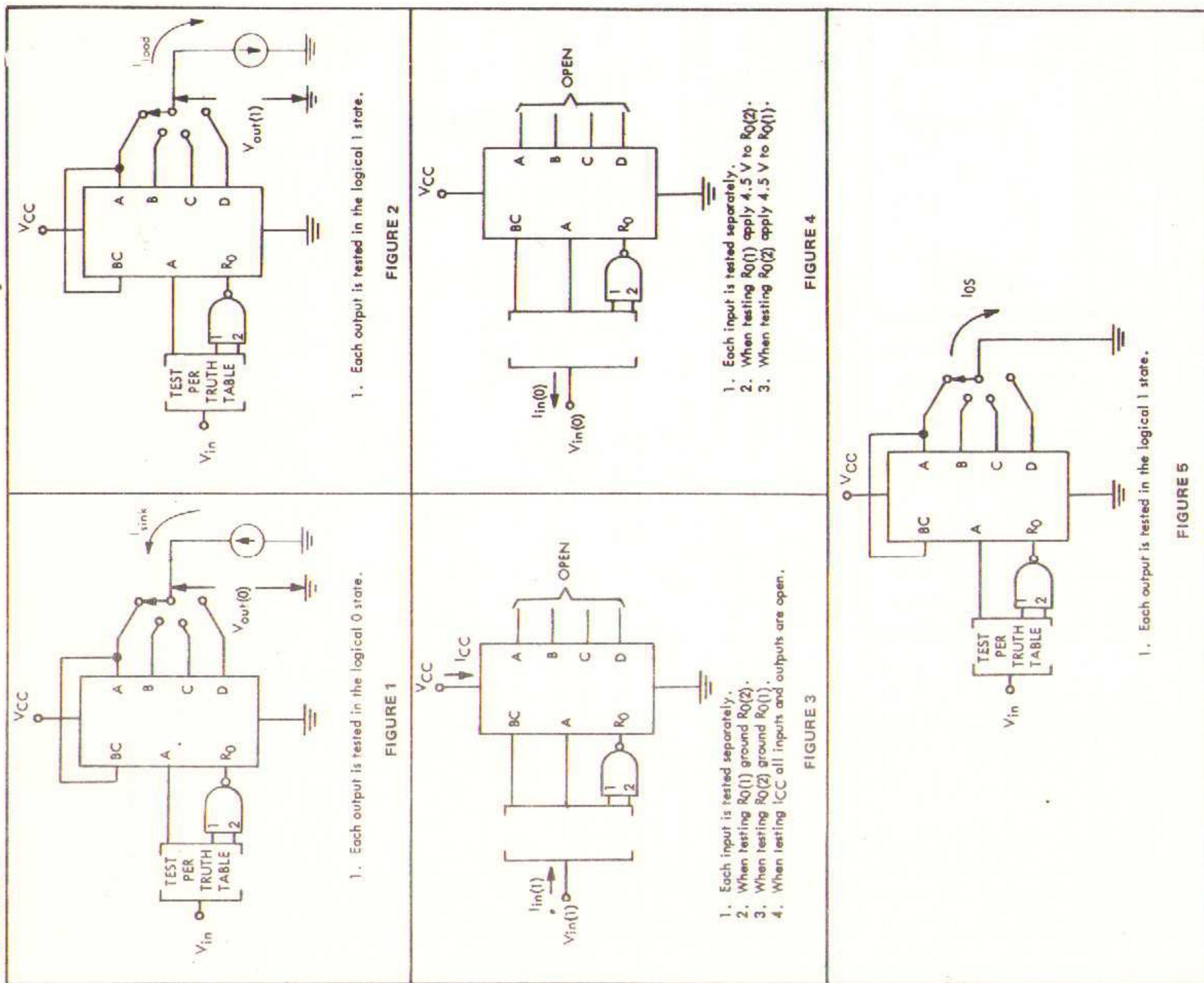


FIGURE 6-SWITCHING TIMES

Logic

TRUTH TABLE (See Notes 1 thru 3)

t _H INPUT	t _H +1 INPUT			OUTPUT
	A1	A2	B	
1	1	0	1	Inhibit
0	X	1	0	Inhibit
X	0	1	X	0
0	X	0	0	Inhibit
X	0	0	X	One Shot
1	1	1	0	One Shot
1	1	1	1	One Shot
0	X	0	0	Inhibit
0	X	0	1	Inhibit
0	X	1	1	Inhibit
1	1	0	0	Inhibit
1	1	0	1	Inhibit

1 = V_{in(1)} ≥ 2 V
0 = V_{in(0)} ≤ 0.8 V

- NOTES: 1. t_H = time before input transition.
2. t_H + 1 = time after input transition.
3. X Indicates that either a logical 0 or 1, may be present.
4. NC = No Internal Connection.

description

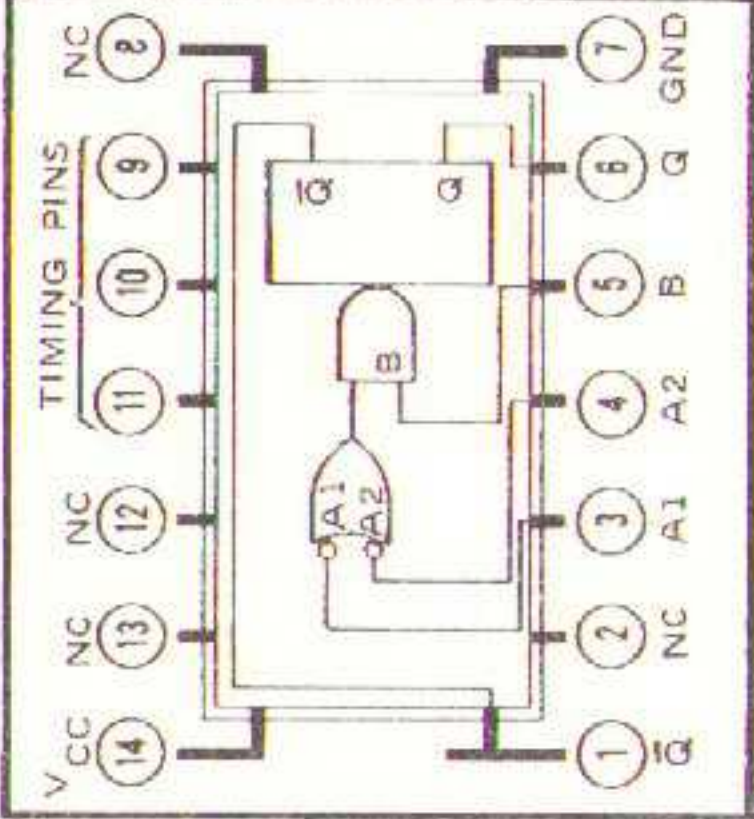
This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL compatible and featuring temperature-independent backlash, See Figure 1) for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

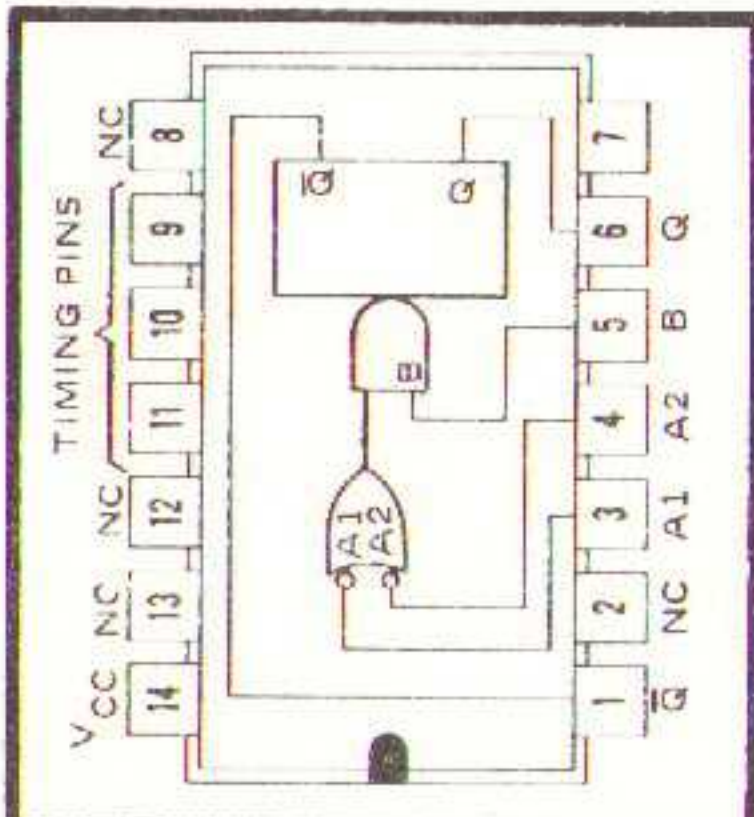
Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin 9 connected to pin 14, pin 10 open) an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

S FLAT PACKAGE (TOP VIEW)
(SEE NOTES 6 THRU 9)

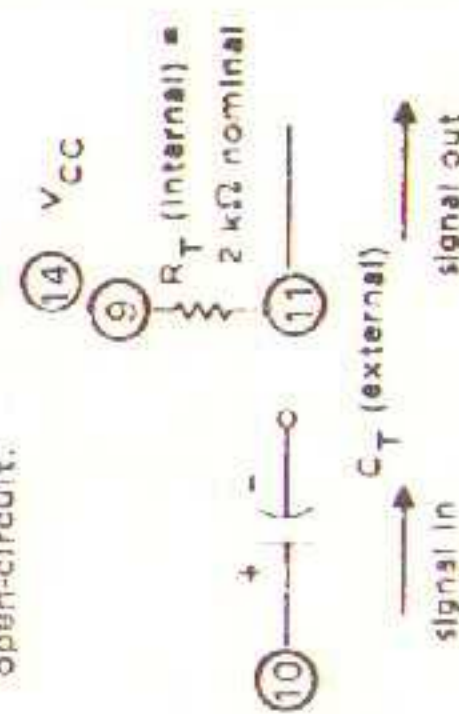


J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)
(SEE NOTES 6 THRU 9)



positive logic: see truth table and notes 5 and 6

- A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
- B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
- To obtain variable pulse width connect external variable resistance between pin 9 and pin 14. No external current limiting is needed.
- For accurate repeatable pulse widths connect an external resistor between pin 11 and pin 12 with pin 9 open-circuit.



description (continued)

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_2 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

recommended operating conditions

Supply Voltage V _{CC} :	SN54121 Circuits	SN74121 Circuits
Normalized Fan-Out From Each Output, N	10	10
Input Pulse Rise/Fall Time:	Schmitt Input (B)	Schmitt Input (B)
Logic Inputs (A1, A2)	1	1
Input Pulse Width	50 ns	50 ns
External Timing Resistance Between Pins 11 and 14 (Pin 9 open)	1.4 kΩ	1.4 kΩ
External Timing Resistance: SN54121	30 kΩ	30 kΩ
SN74121	40 kΩ	40 kΩ
Timing Capacitance	0	1000 μF
Output Pulse Width	40 s	40 s
Duty Cycle: R _T = 2 kΩ	67%	67%
R _T = 30 kΩ (SN54121) or R _T = 40 kΩ (SN74121)	90%	90%

IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible. TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

electrical characteristics over operating free-air temperature range

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
V_{T+} Positive-going threshold voltage at A input	57	$V_{CC} = \text{MIN}$		1.4	2	V
V_{T-} Negative-going threshold voltage at A input	57	$V_{CC} = \text{MIN}$	0.8	1.4		V
V_{T+} Positive-going threshold voltage at B input	57	$V_{CC} = \text{MIN}$		1.55	2	V
V_{T-} Negative-going threshold voltage at B input	57	$V_{CC} = \text{MIN}$	0.8	1.35		V
$V_{out(0)}$ Logical 0 output voltage	57	$V_{CC} = \text{MIN}$, $I_{\text{sink}} = 16 \text{ mA}$		0.22	0.4	V
$V_{out(1)}$ Logical 1 output voltage	57	$V_{CC} = \text{MIN}$, $I_{\text{load}} = -400 \mu\text{A}$	2.4	3.3		V
$I_{in(0)}$ Logical 0 level input current at A1 or A2	58	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$		-1	-1.6	mA
$I_{in(0)}$ Logical 0 level input current at B	59	$V_{CC} = \text{MAX}$, $V_{in} = 0.4 \text{ V}$		-2	-3.2	mA
$I_{in(1)}$ Logical 1 level input current at A1 or A2	60	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$		2	40	μA
$I_{in(1)}$ Logical 1 level input current at A1 or A2	60	$V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$		0.05	1	mA
$I_{in(1)}$ Logical 1 level input current at B	61	$V_{CC} = \text{MAX}$, $V_{in} = 2.4 \text{ V}$		4	80	μA
$I_{in(1)}$ Logical 1 level input current at B	61	$V_{CC} = \text{MAX}$, $V_{in} = 5.5 \text{ V}$		0.05	1	mA
I_{OS} Short circuit output current at Q or $\bar{Q}$ §	62 and 63	$V_{CC} = \text{MAX}$	-20	-25	-55	mA
I_{CC} Power supply current in quiescent (unfired) state	64	$V_{CC} = \text{MAX}$	-18	-25	-55	mA
I_{CC} Power supply current in fired state	64	$V_{CC} = \text{MAX}$		13	25	mA
I_{CC} Power supply current in fired state	64	$V_{CC} = \text{MAX}$		23	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1} Propagation delay time to logical 1 level from B input to Q output	72	$C_L = 15 \text{ pF}$, $C_T = 80 \text{ pF}$	15	35	55	ns
t_{pd1} Propagation delay time to logical 1 level from A1/A2 inputs to Q output	72	$C_L = 15 \text{ pF}$, $C_T = 80 \text{ pF}$	25	45	70	ns
t_{pd0} Propagation delay time to logical 0 level from B input to Q output	72	$C_L = 15 \text{ pF}$, $C_T = 80 \text{ pF}$	20	40	65	ns
t_{pd0} Propagation delay time to logical 0 level from A1/A2 inputs to Q output	72	$C_L = 15 \text{ pF}$, $C_T = 80 \text{ pF}$	30	50	80	ns
$t_{p(out)}$ Pulse width obtained using internal timing resistor	73	$C_L = 15 \text{ pF}$, $R_T = \text{Open}$, $C_T = 80 \text{ pF}$, Pin ③ to V_{CC}	70	110	150	ns
$t_{p(out)}$ Pulse width obtained with zero timing capacitance	73	$C_L = 15 \text{ pF}$, $R_T = \text{Open}$, $C_T = 0$, Pin ③ to V_{CC}	20	30	50	ns
$t_{p(out)}$ Pulse width obtained using external timing resistor	73	$C_L = 15 \text{ pF}$, $R_T = 10 \text{ k}\Omega$, $C_T = 100 \text{ pF}$, Pin ③ to V_{CC}	600	700	800	ns
$t_{p(out)}$ Pulse width obtained using external timing resistor	73	$C_L = 15 \text{ pF}$, $R_T = 10 \text{ k}\Omega$, $C_T = 1 \mu\text{F}$, Pin ③ to V_{CC}	6	7	8	ms
t_{hold} Minimum duration of trigger pulse	73	$C_L = 15 \text{ pF}$, $R_T = \text{Open}$, $C_T = 80 \text{ pF}$, Pin ③ to V_{CC}		30	50	ns

§ Unless otherwise noted data is applicable for SN54121 and SN74121.

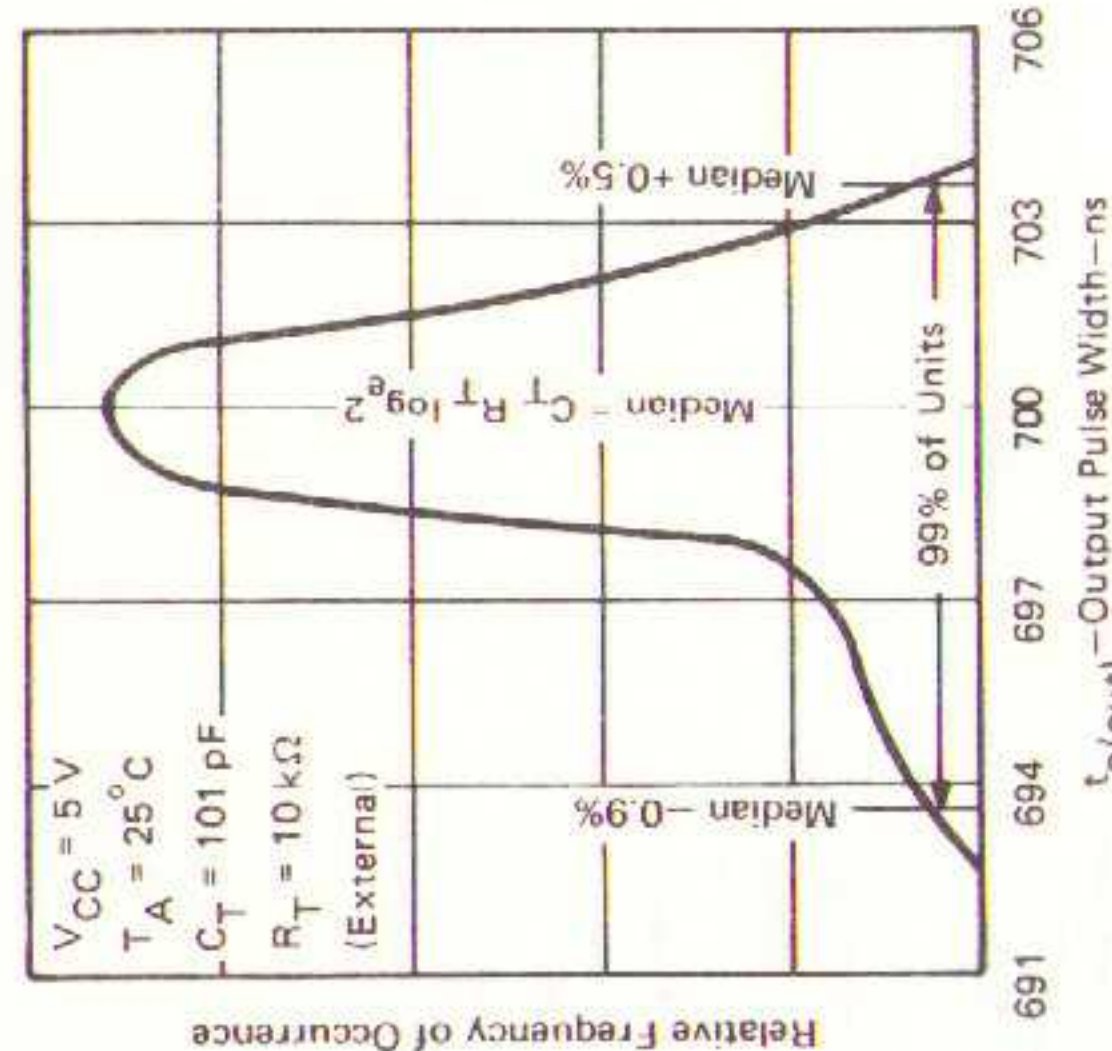
DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

FIGURE H

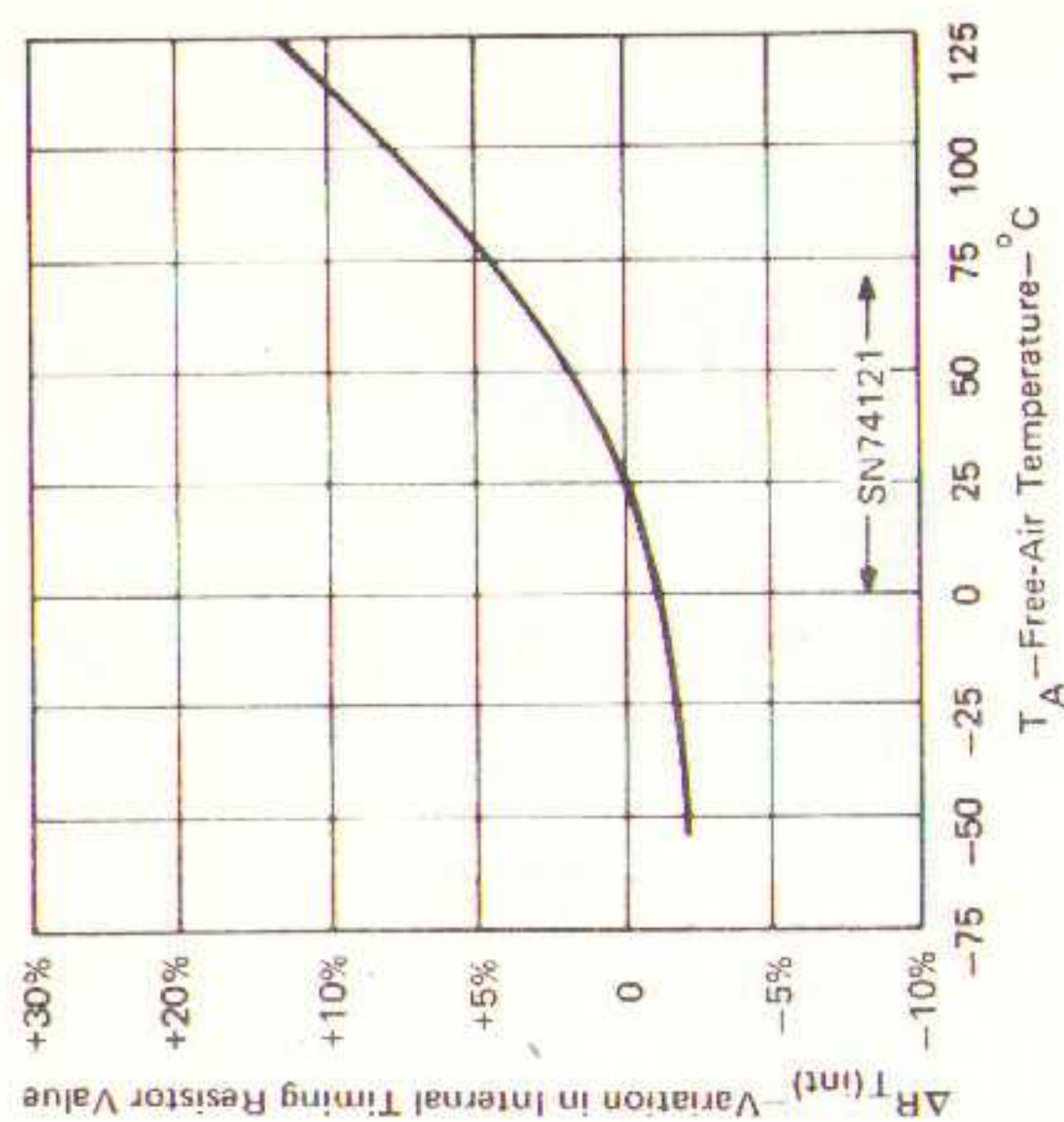
VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE-AIR TEMPERATURE

FIGURE I

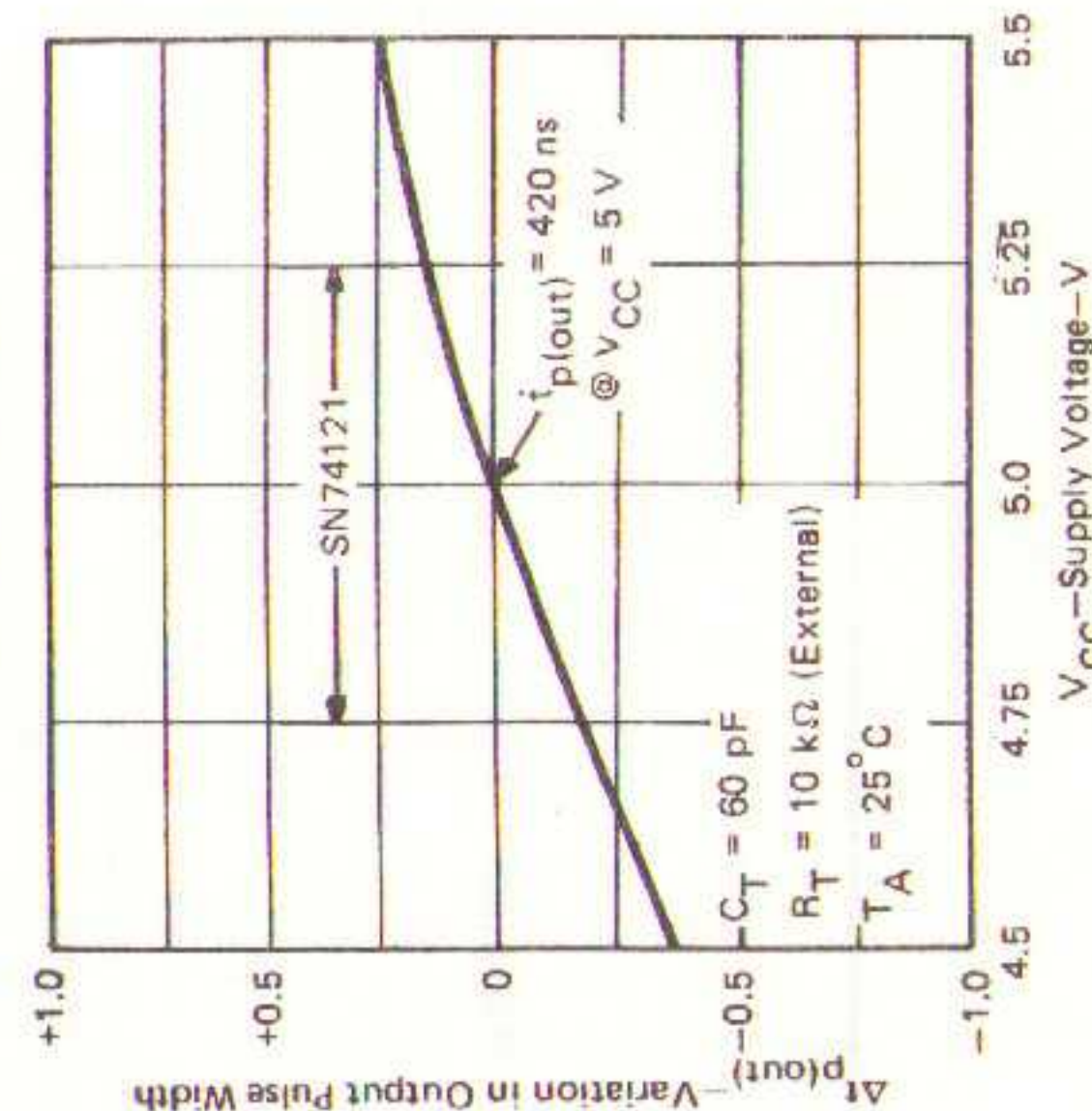
VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

FIGURE J

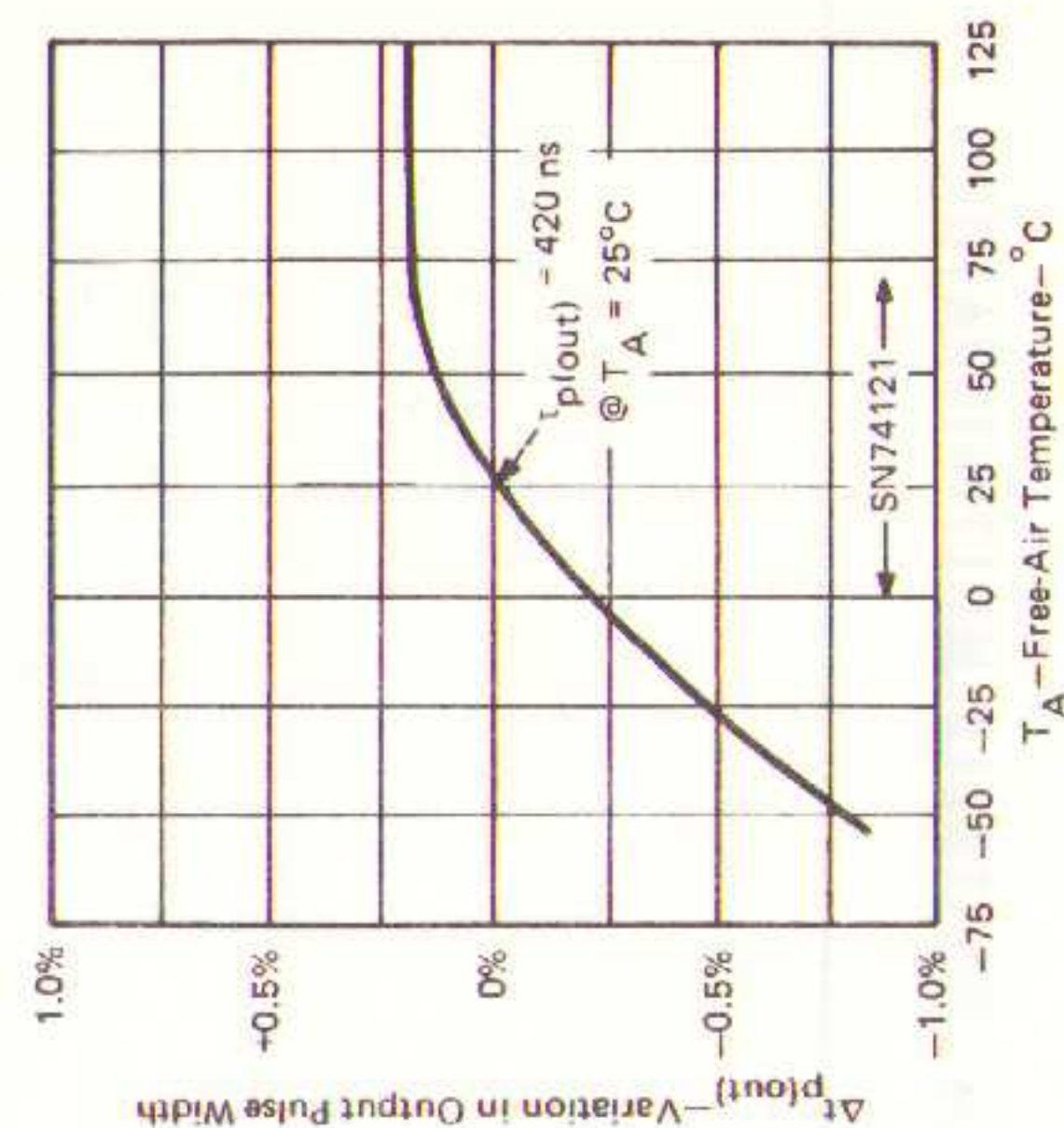
VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

FIGURE K

TYPICAL CHARACTERISTICS

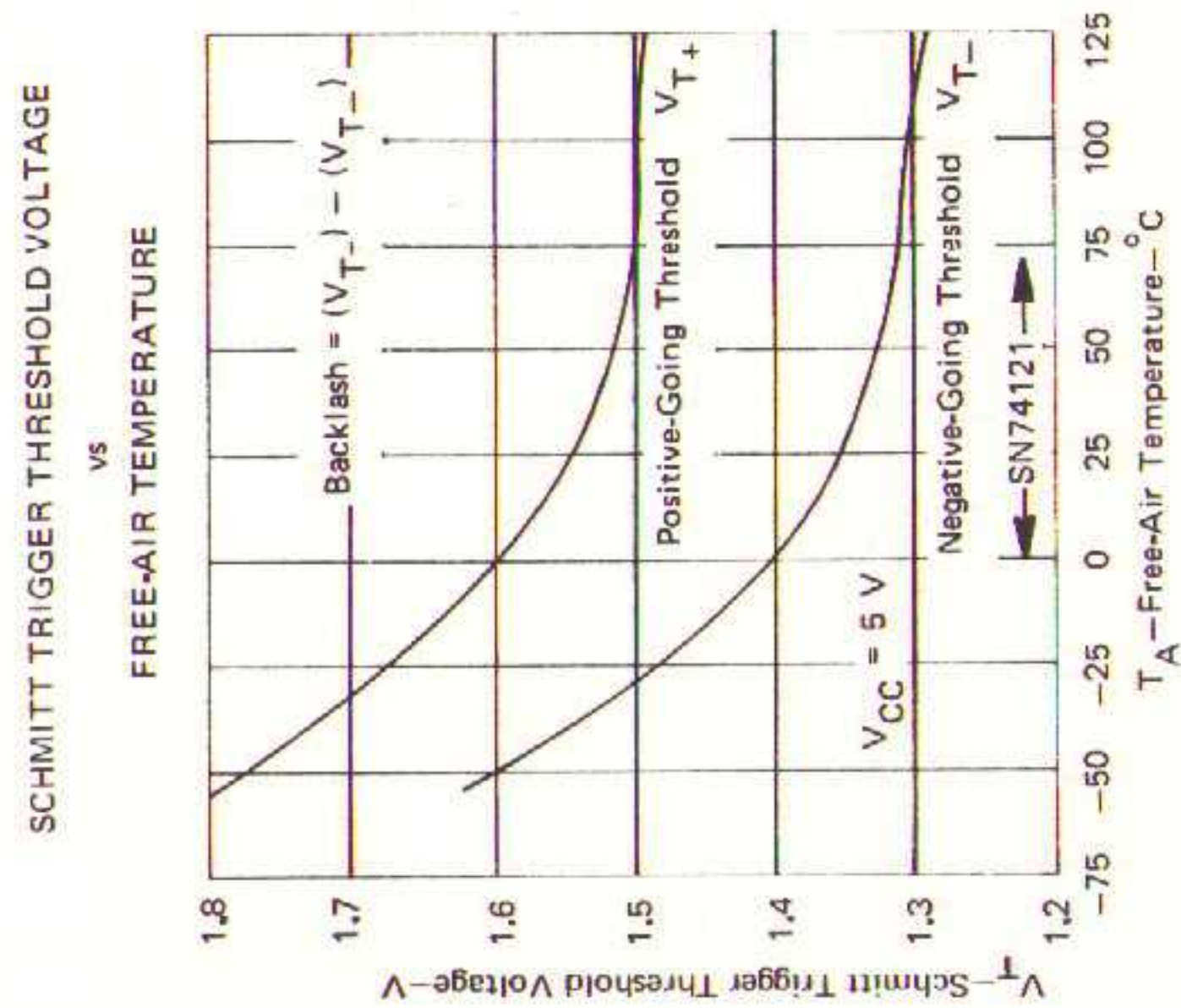


FIGURE L

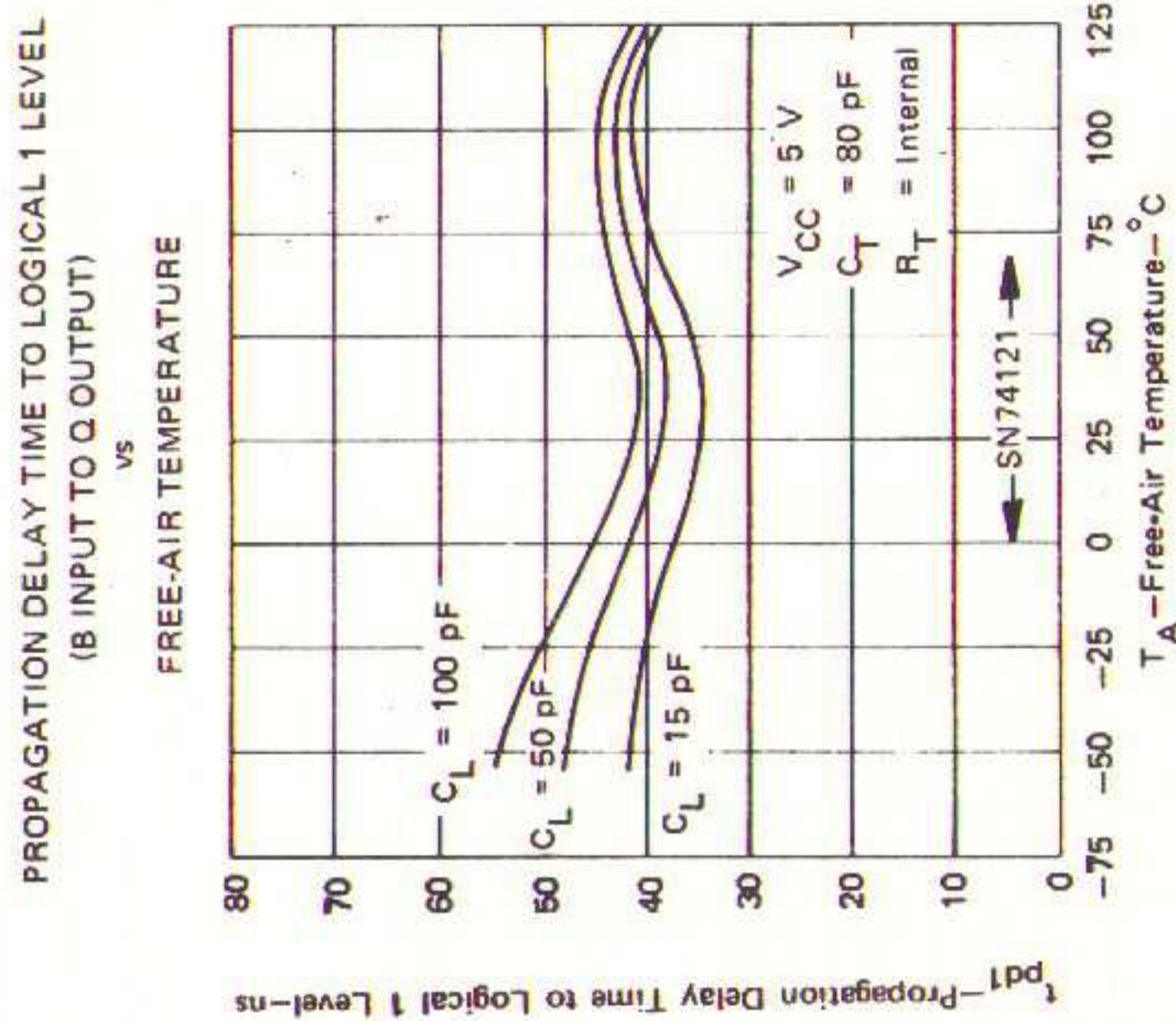


FIGURE M

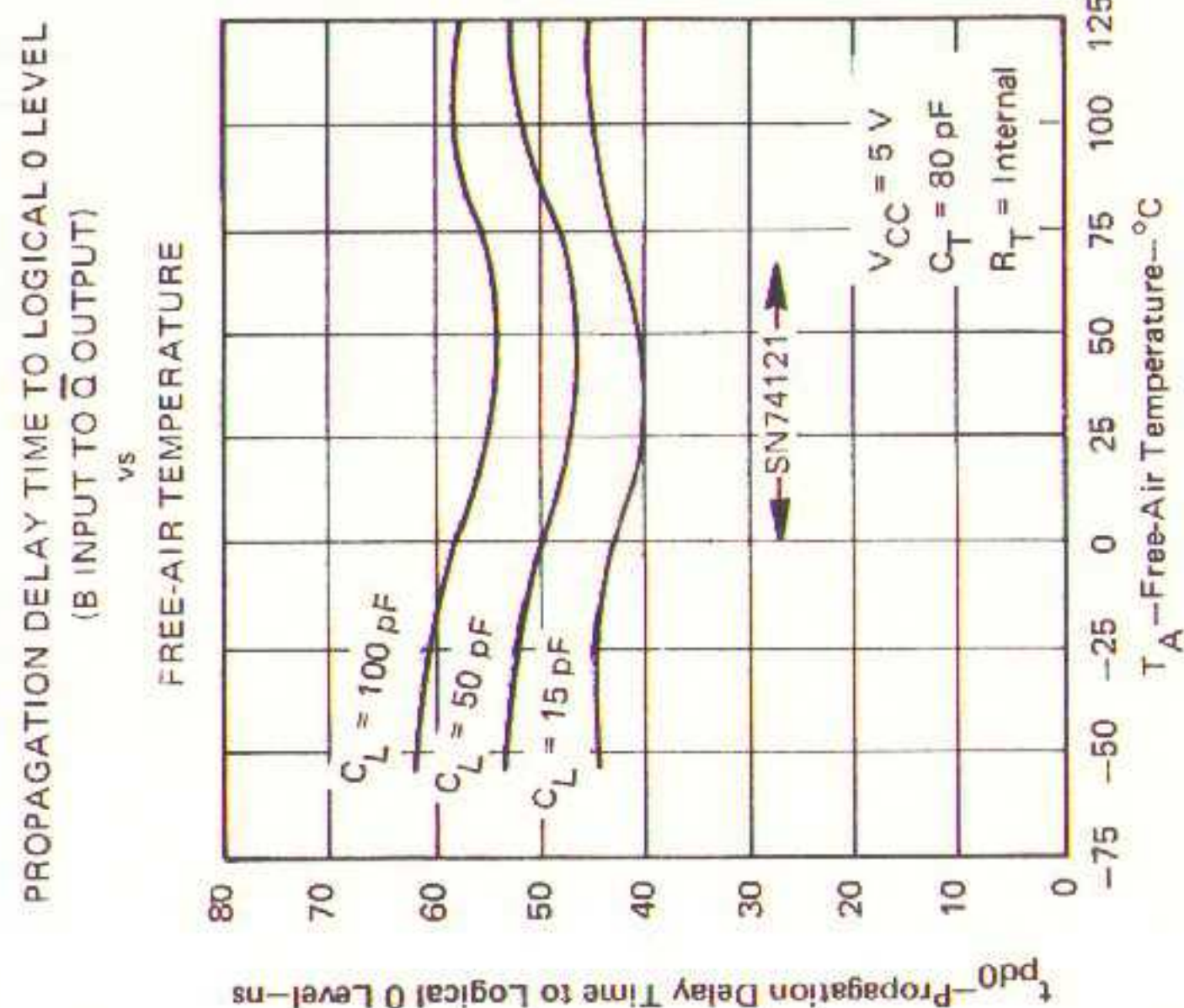


FIGURE N

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

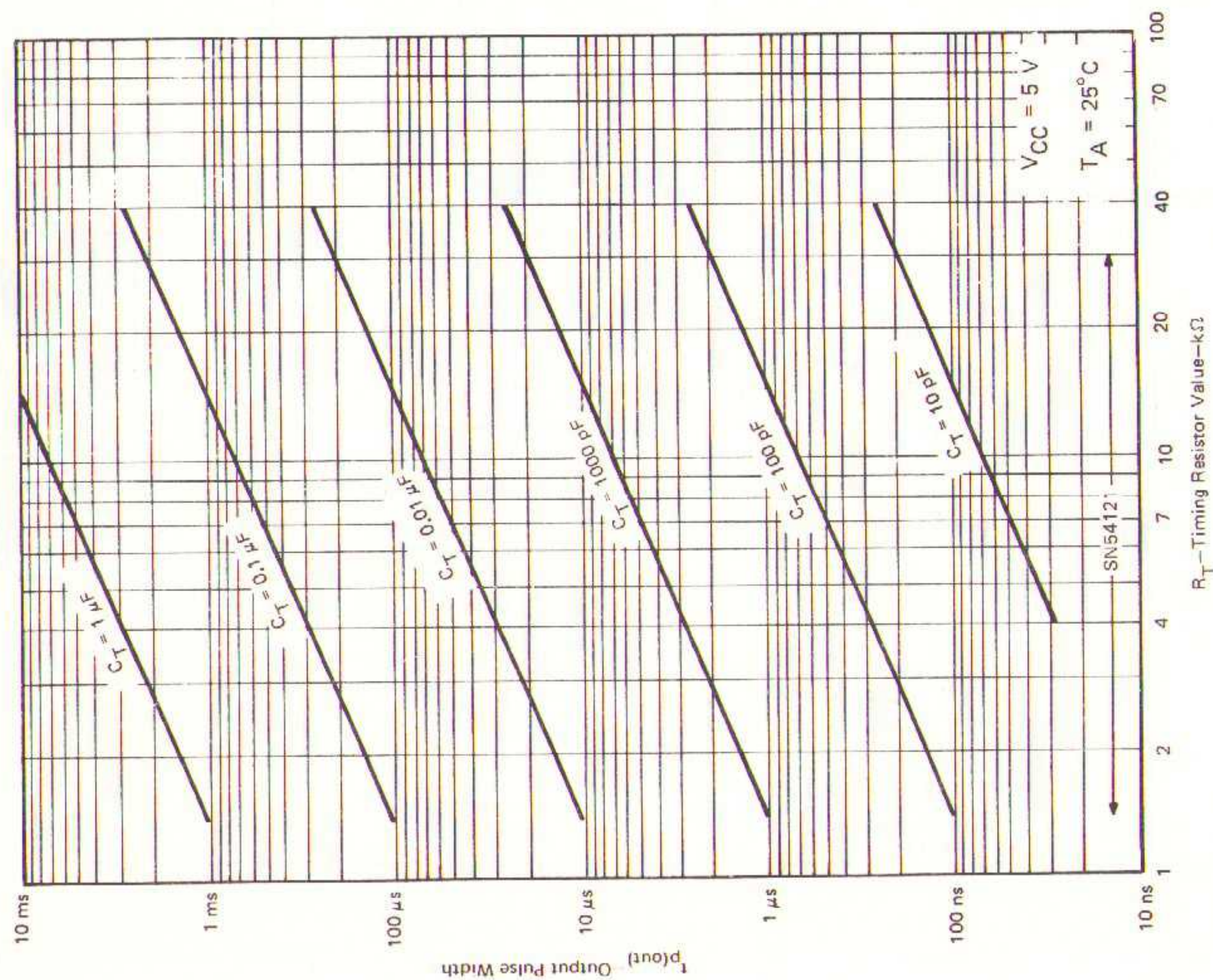


FIGURE O

OUTPUT PULSE WIDTH
vs
EXTERNAL CAPACITANCE

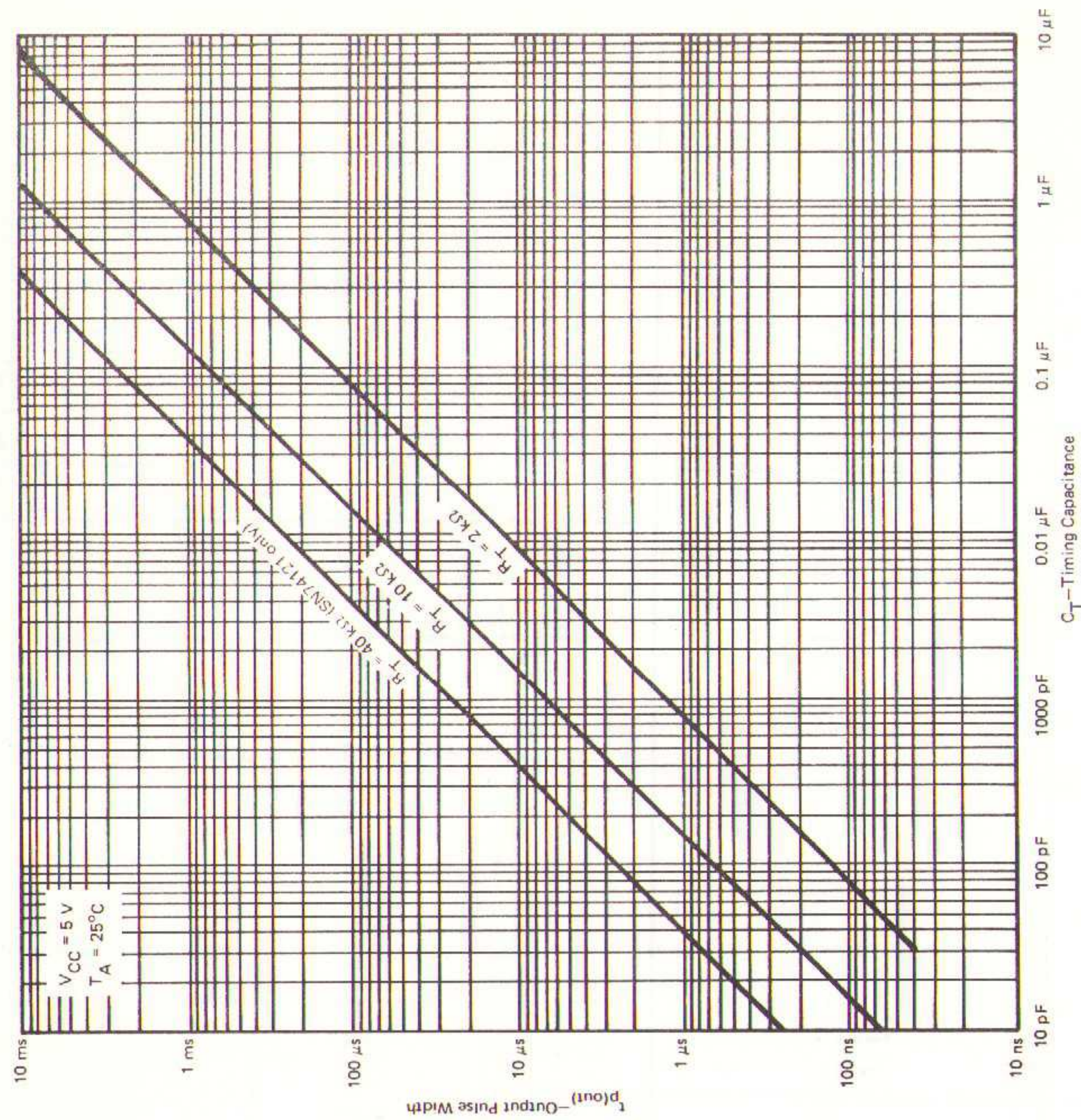
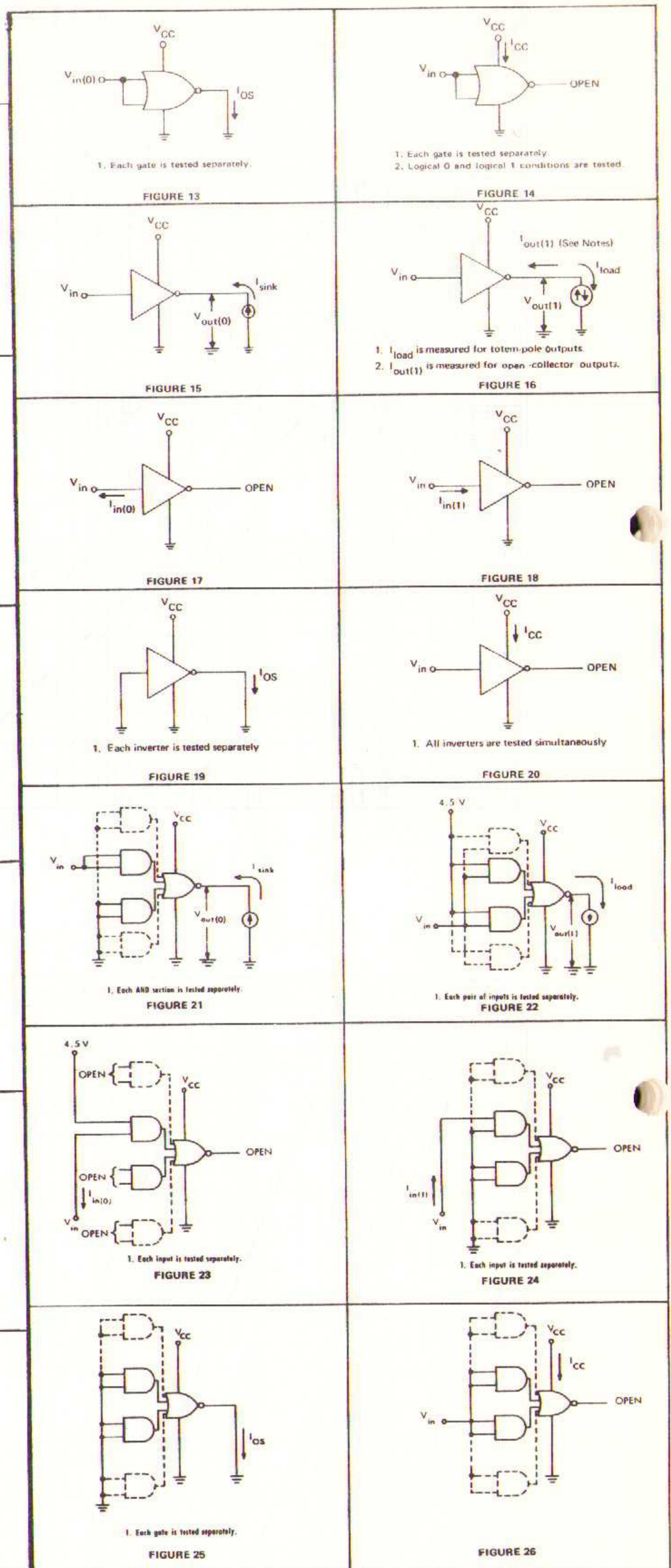
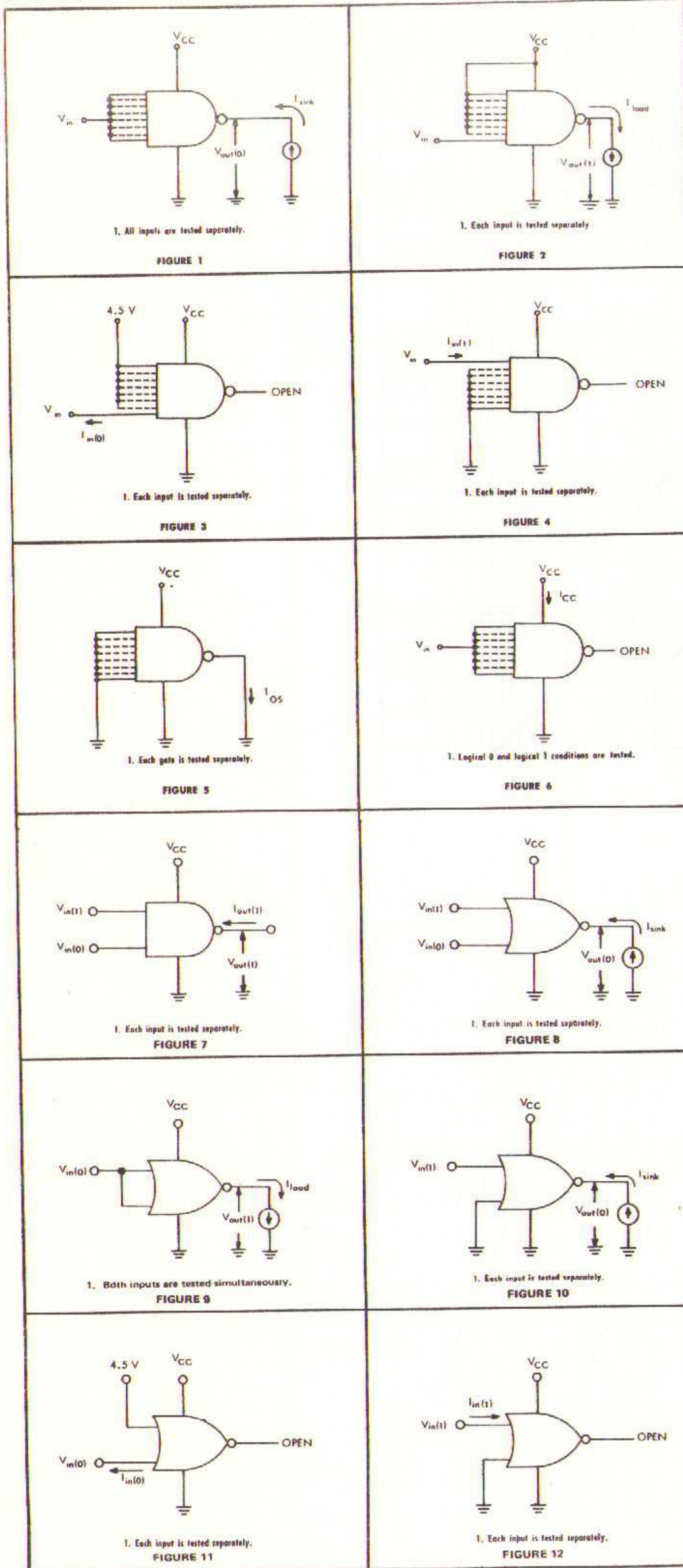


FIGURE P

§Unless otherwise noted data is applicable for SN54121 and SN74121.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



§Arrows indicate actual direction of current flow.

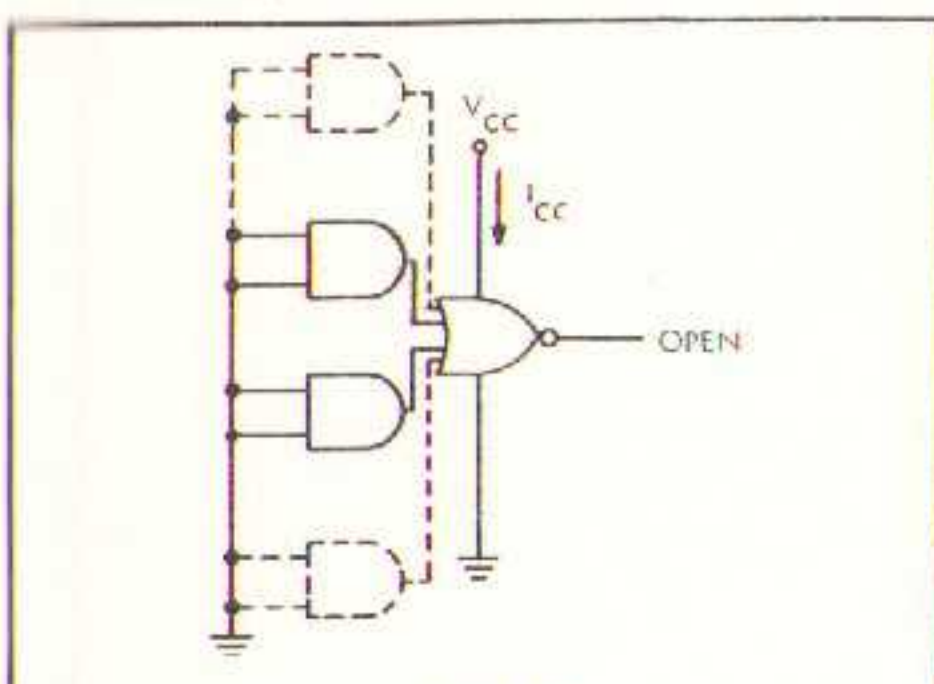


FIGURE 27

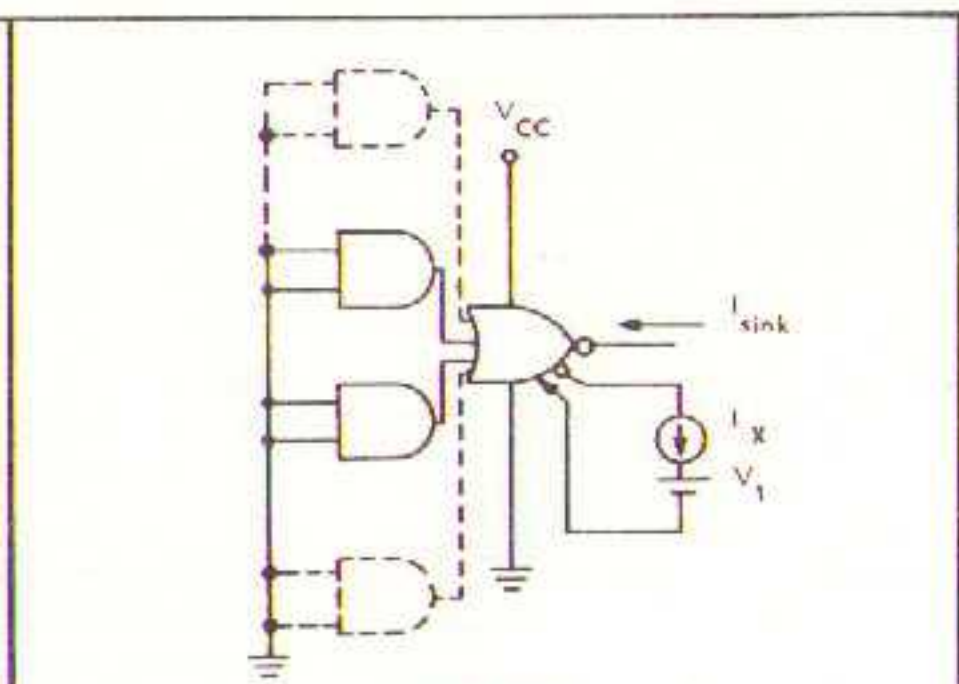


FIGURE 28

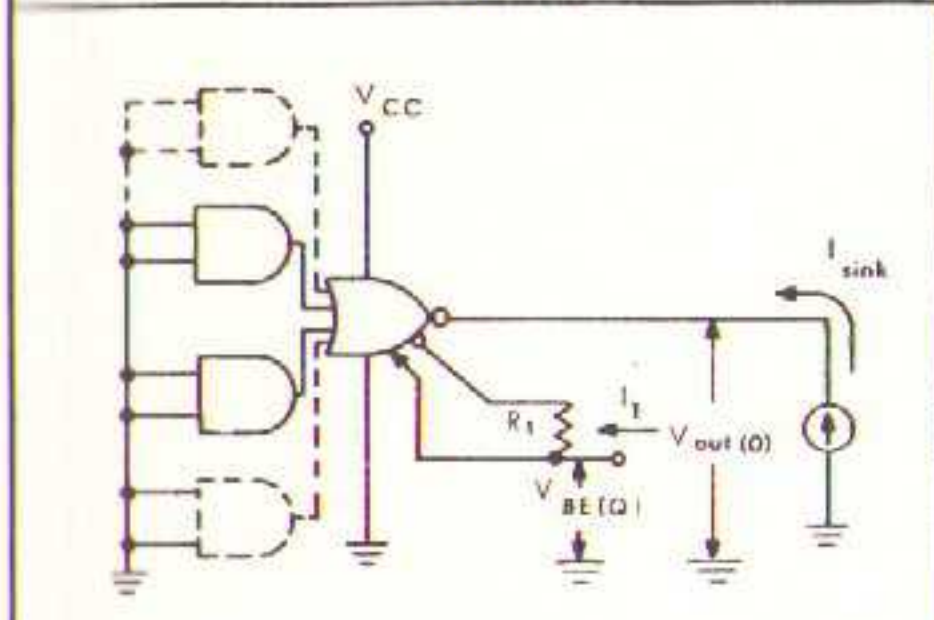


FIGURE 29

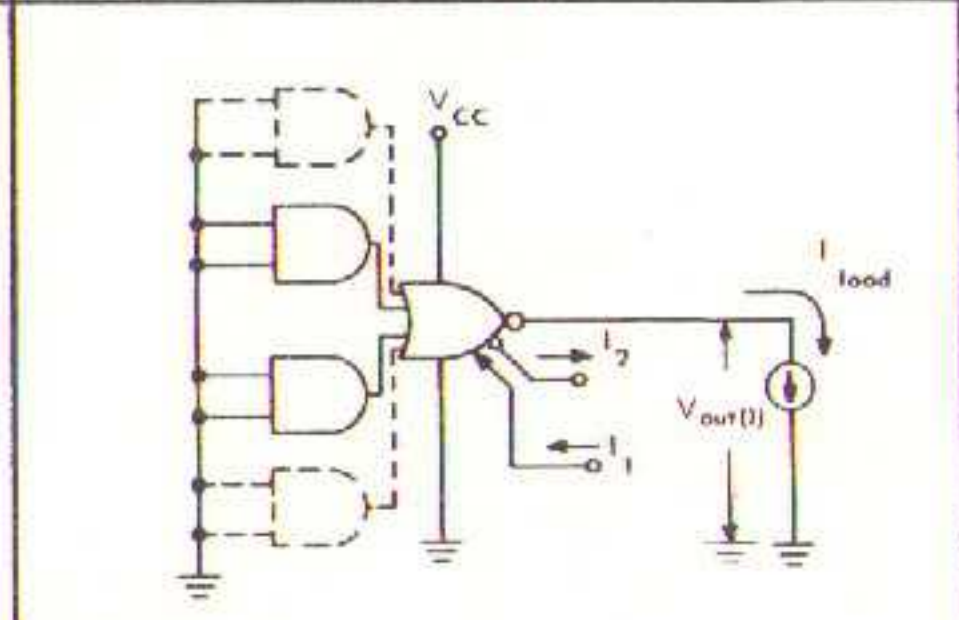


FIGURE 30

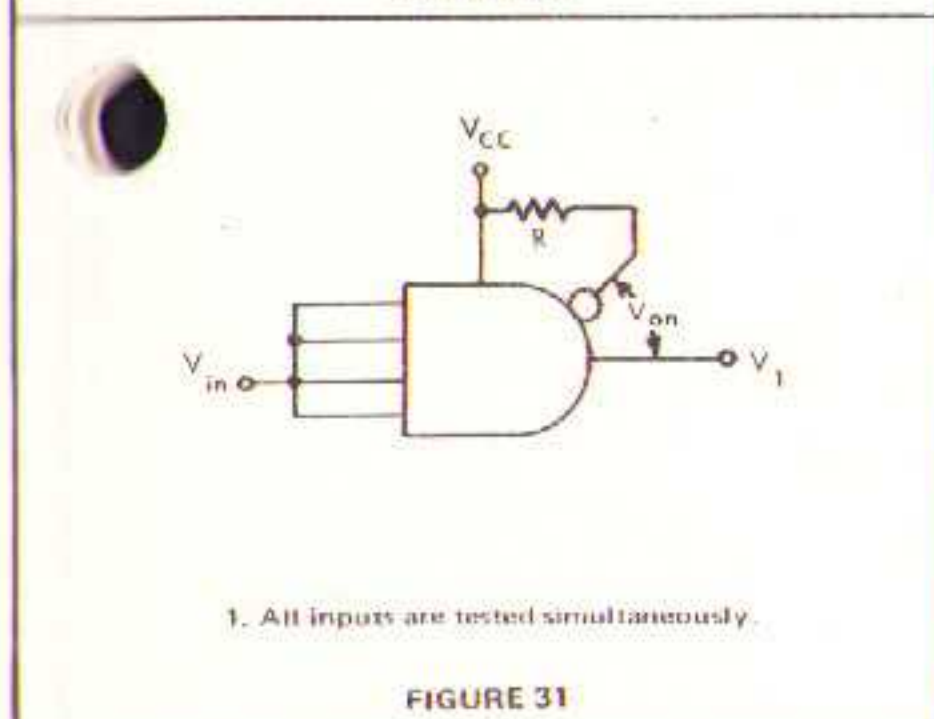


FIGURE 31

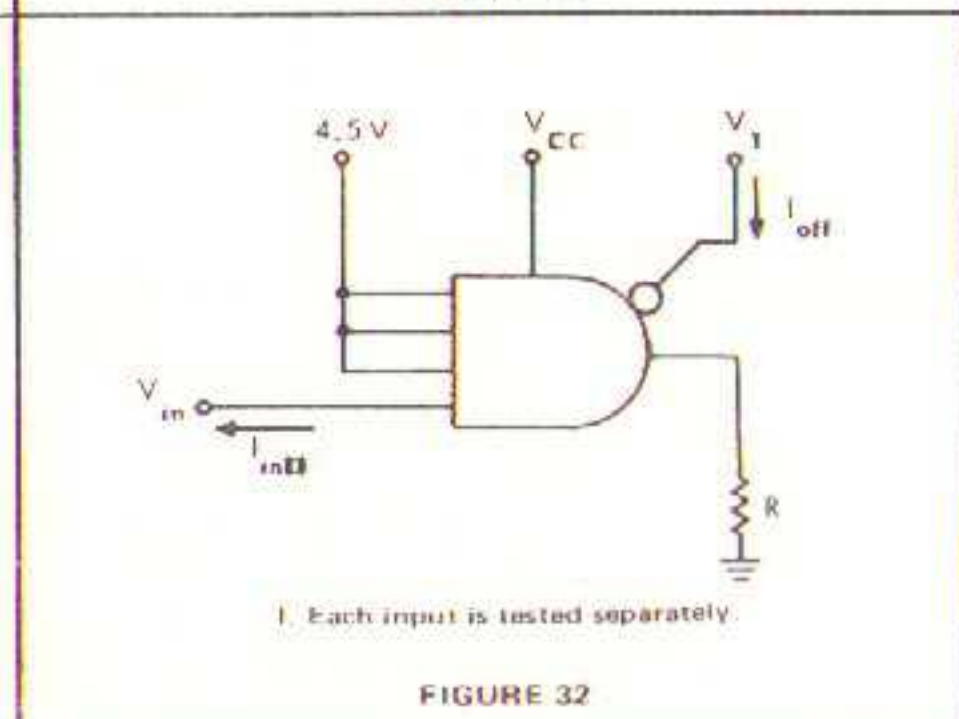


FIGURE 32

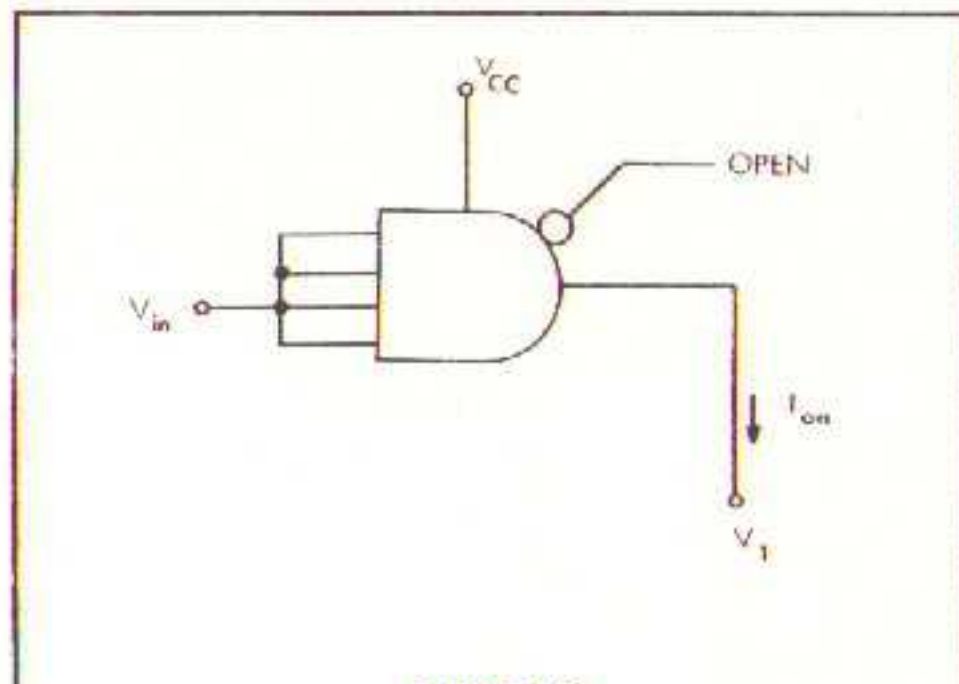


FIGURE 33

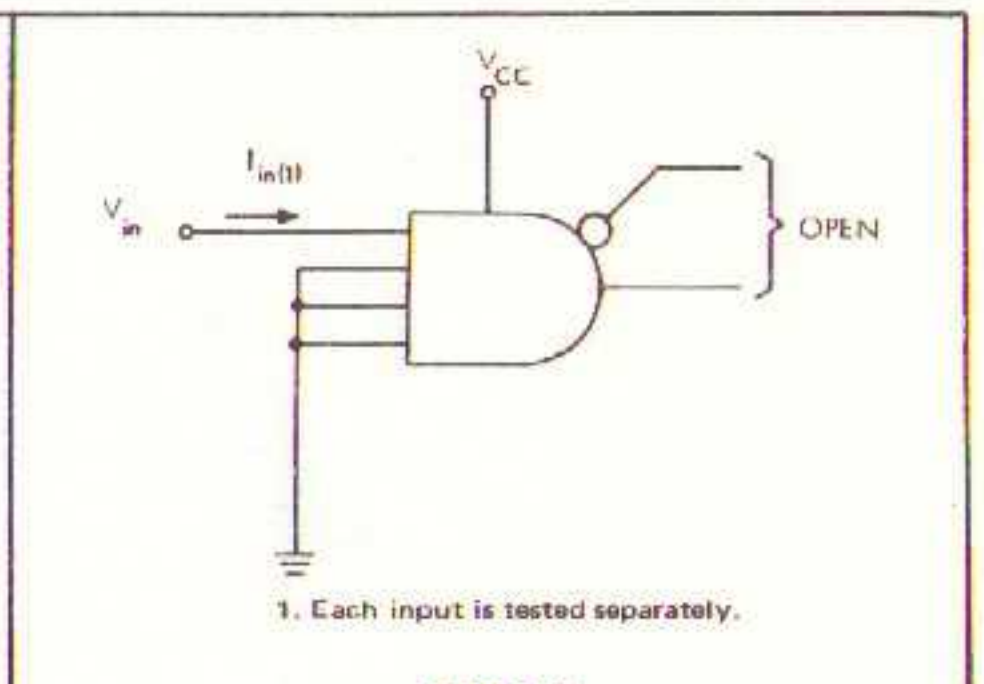
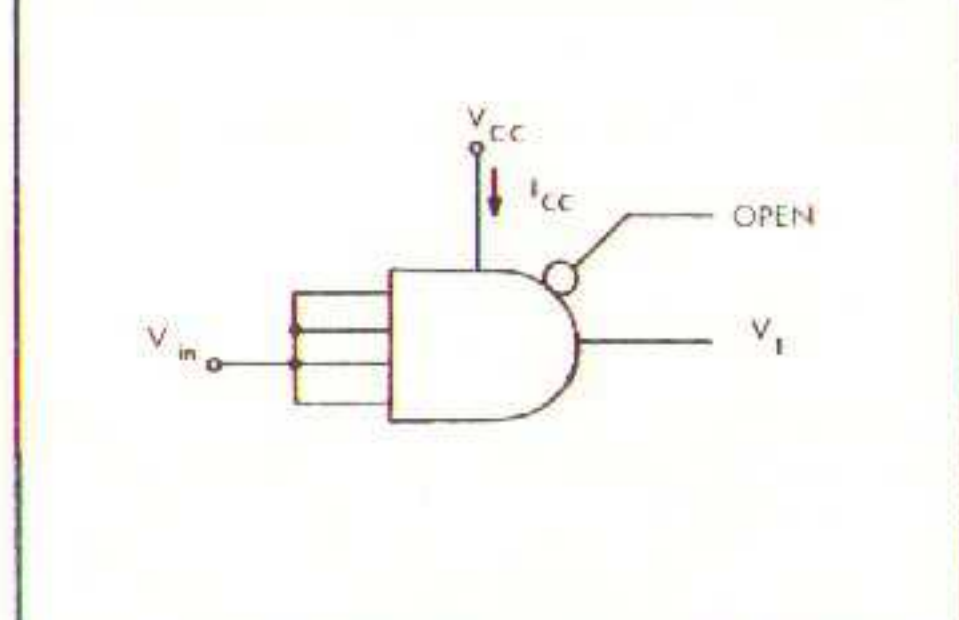
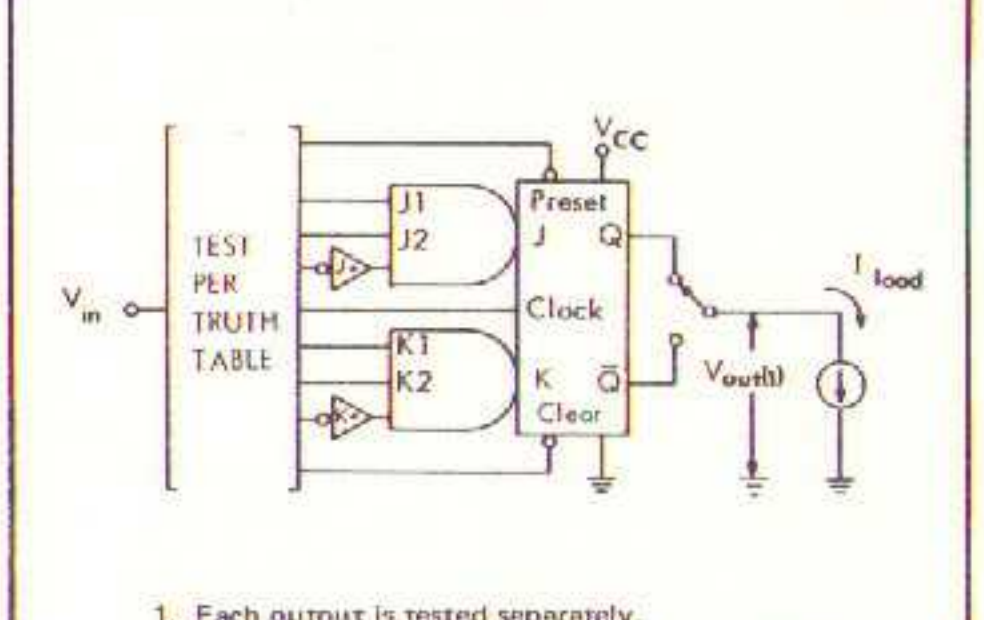


FIGURE 34



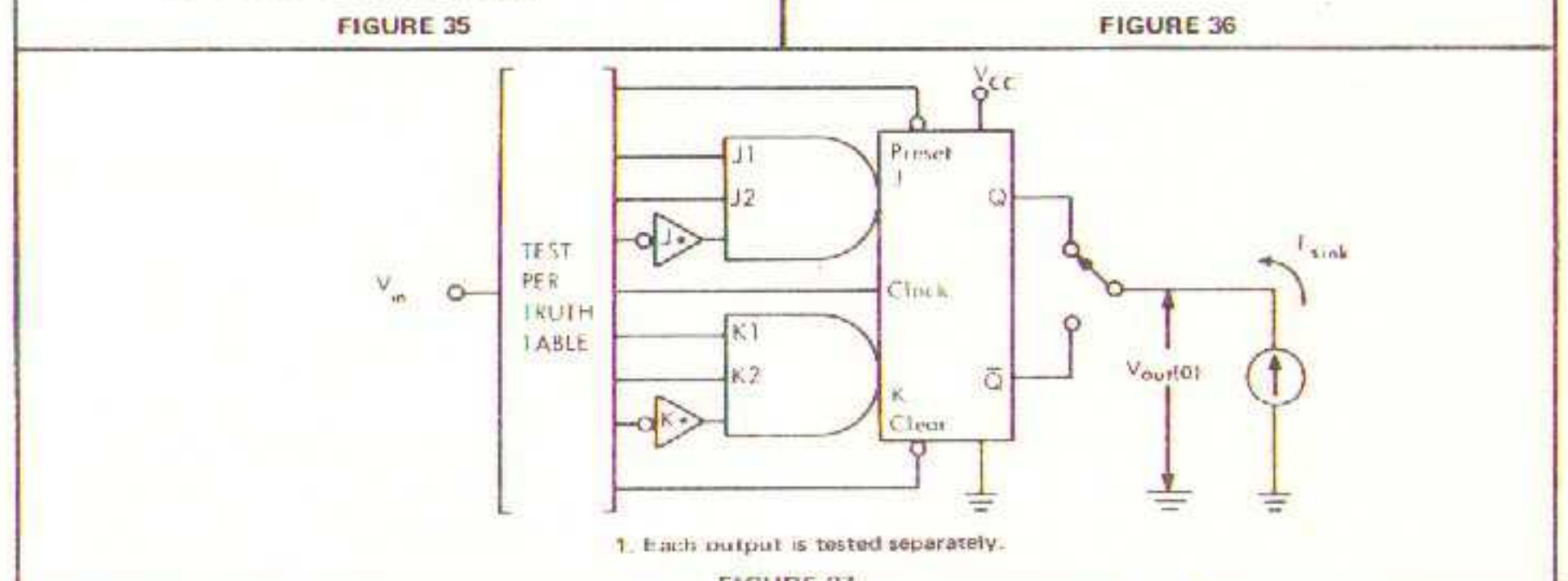
1. "On" and "off" conditions are tested separately.
2. Each gate is tested separately.

FIGURE 35



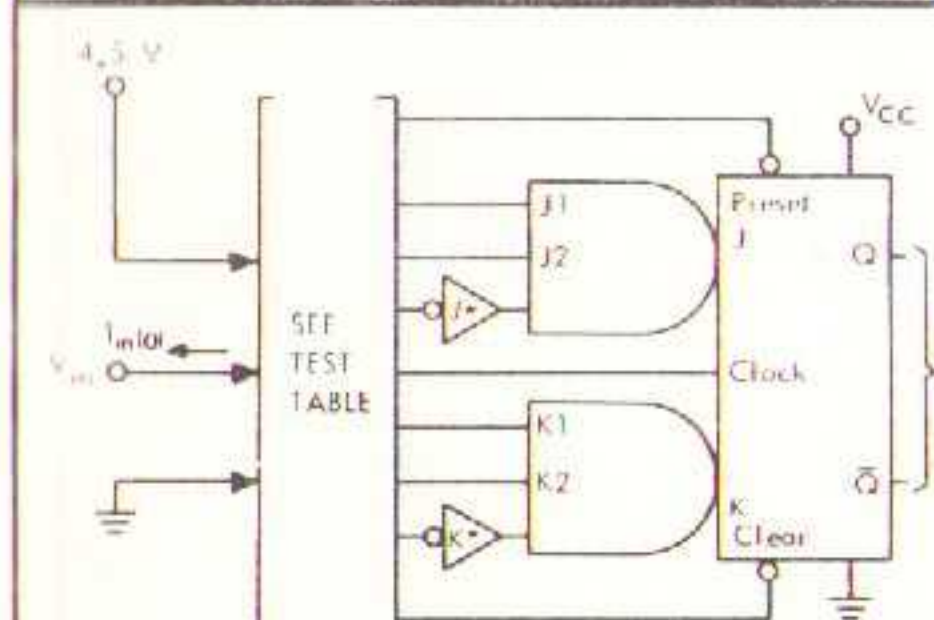
1. Each output is tested separately.
2. Preset and clear are tested with $V_{in(clock)} = 0$.

FIGURE 36



1. Each output is tested separately.

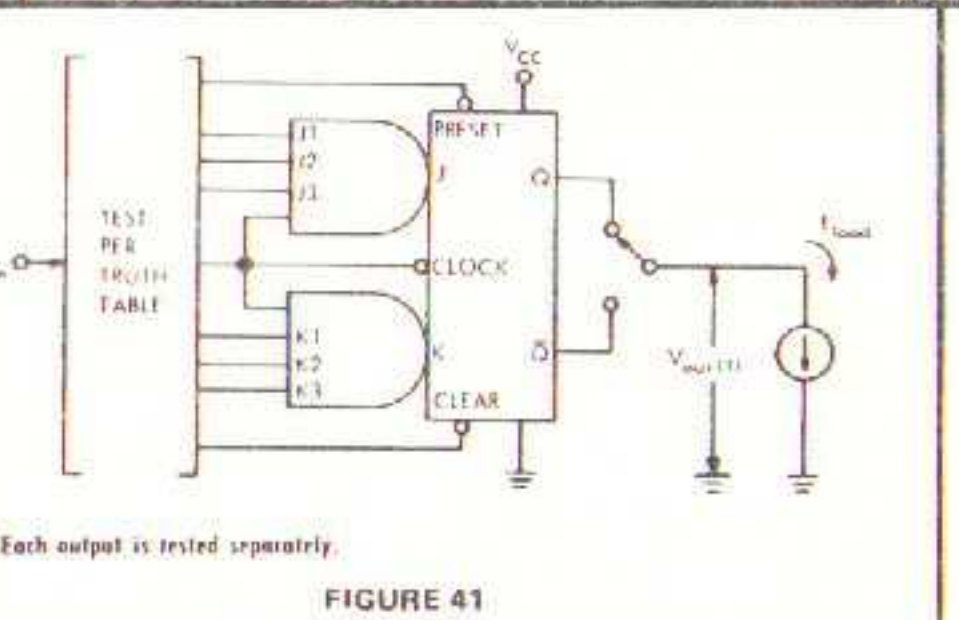
FIGURE 37



1. Each output is tested separately.

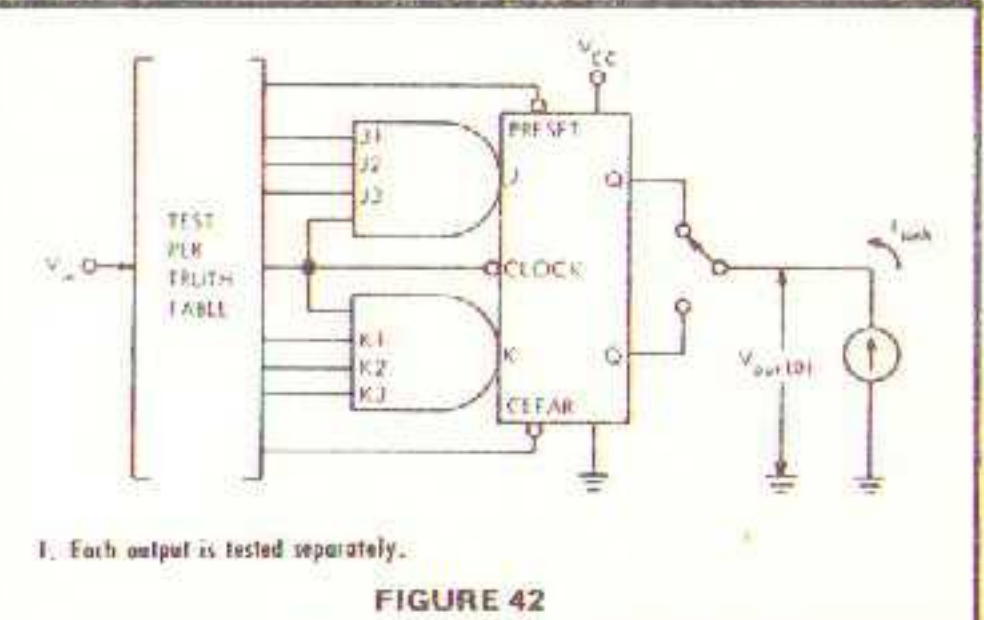
FIGURE 38

TEST TABLE			
Apply V_{in} (Test $I_{in(1)}$)	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J*	Clear
J1	J2	J*	Clear
J*	None	None	None
K2	K1	K*	Preset
K1	K2	K*	Preset
K*	None	None	None
Clock	None	None	None
Preset	K1 and K2	K*	None
Clear	J1 and J2	J*	None



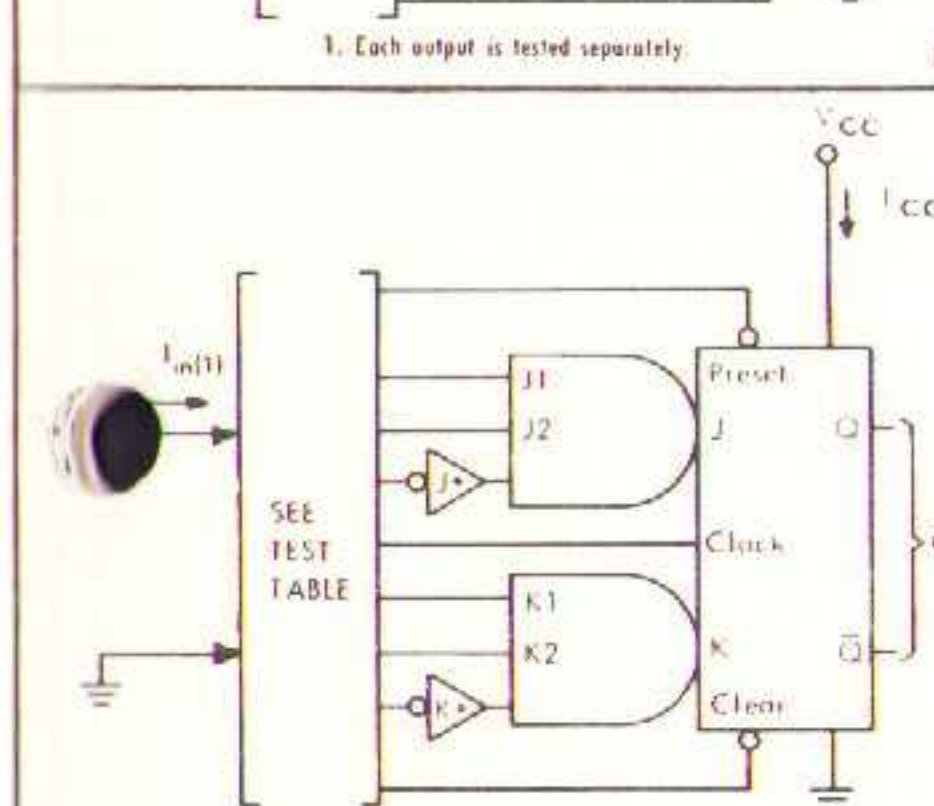
1. Each output is tested separately.

FIGURE 41



1. Each output is tested separately.

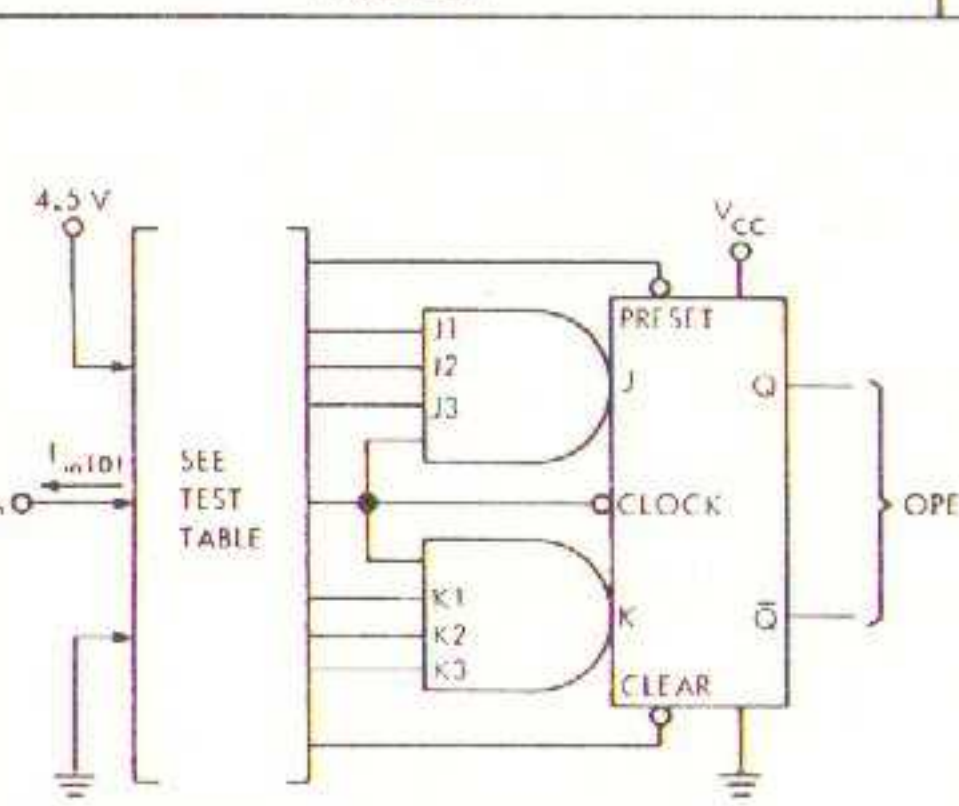
FIGURE 42



1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

FIGURE 39

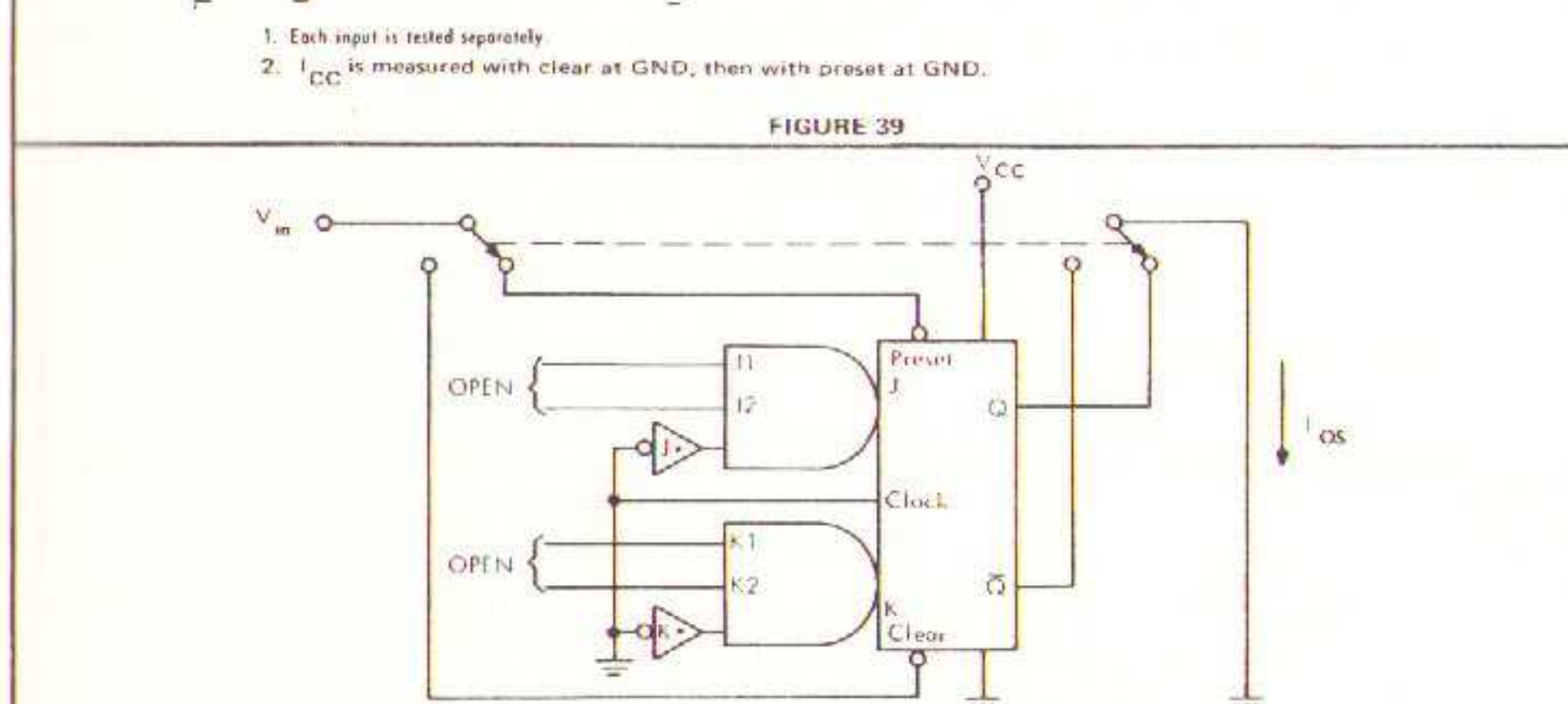
TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
J2	J1 and Clear	J*
J1	J2 and Clear	J*
J*	None	None
K2	K1 and Preset	K*
K1	K2 and Preset	K*
K*	None	None
Clock	None	None
Preset	K1 and K2	K*
Clear	J1 and J2	J*



1. Each input is tested separately.

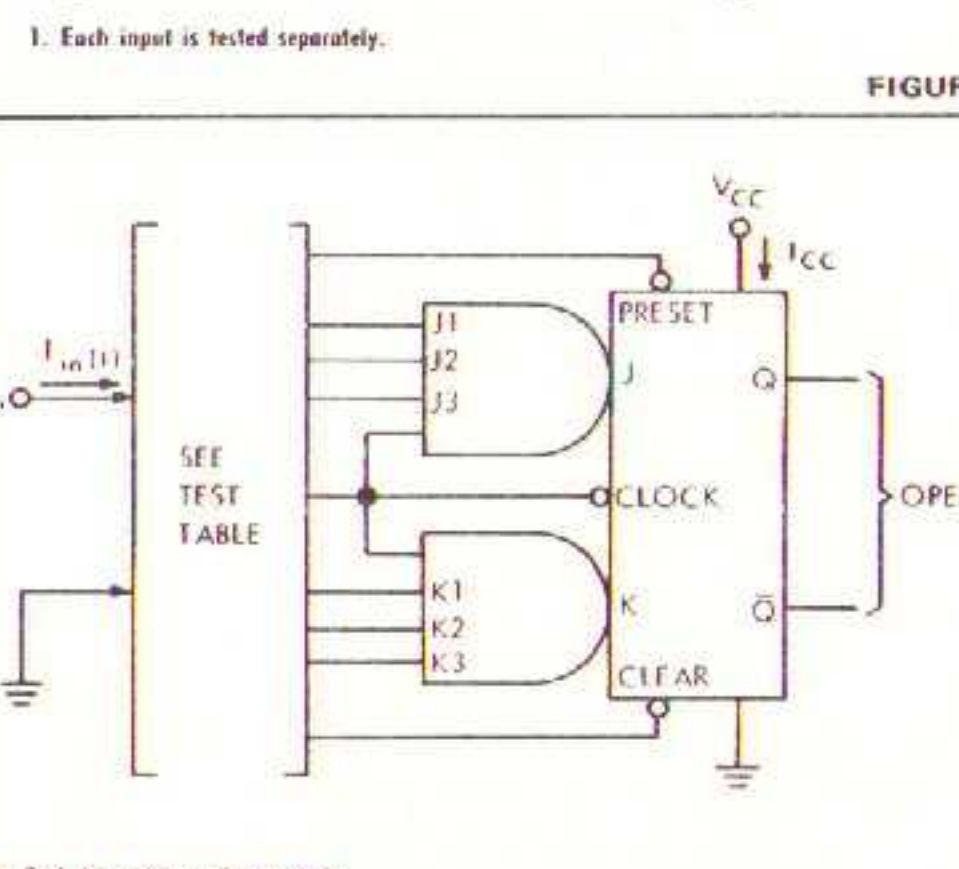
FIGURE 43

TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2



1. Each output is tested separately.

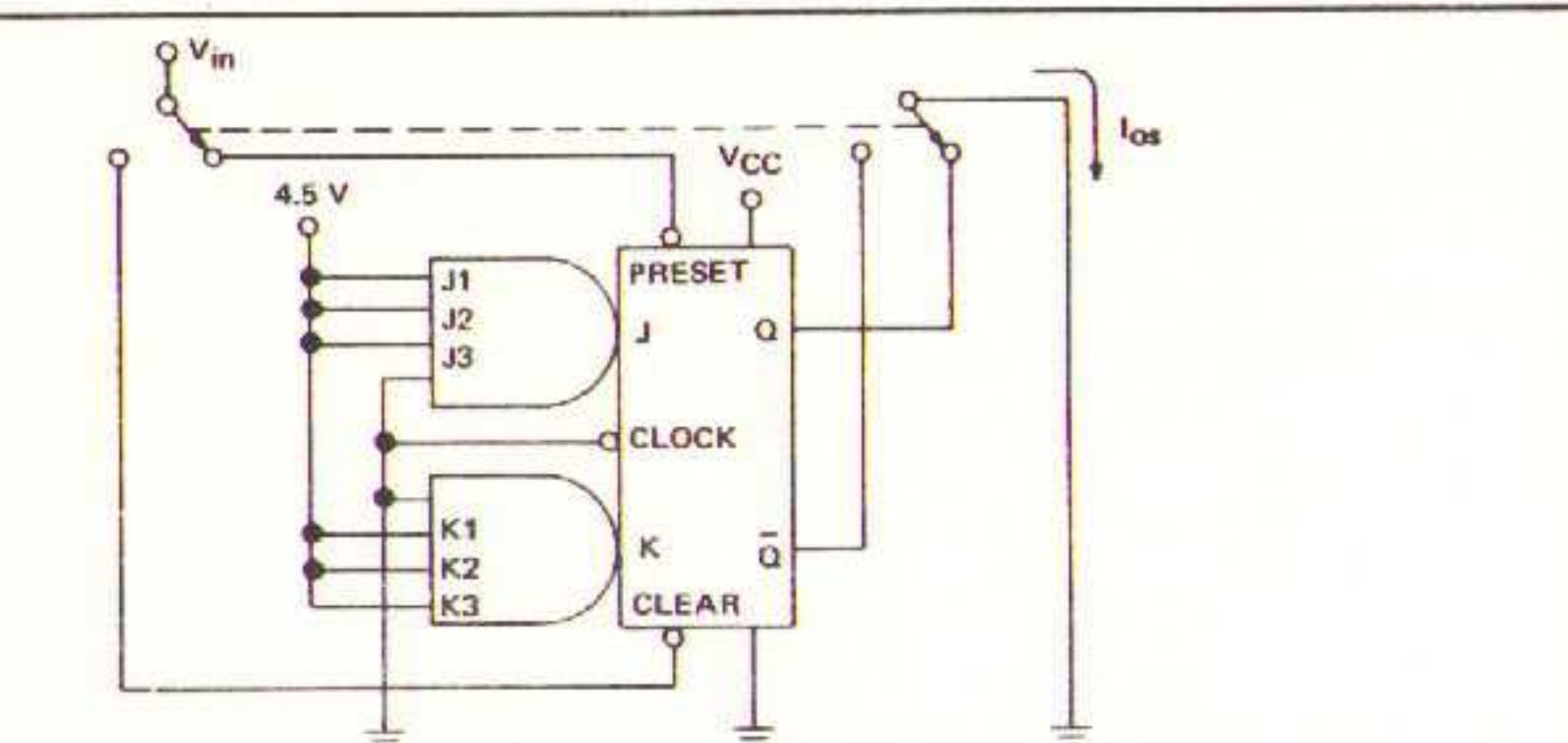
FIGURE 40



1. Each input is tested separately.
2. I_{CC} is measured with clear at GND, then with preset at GND.

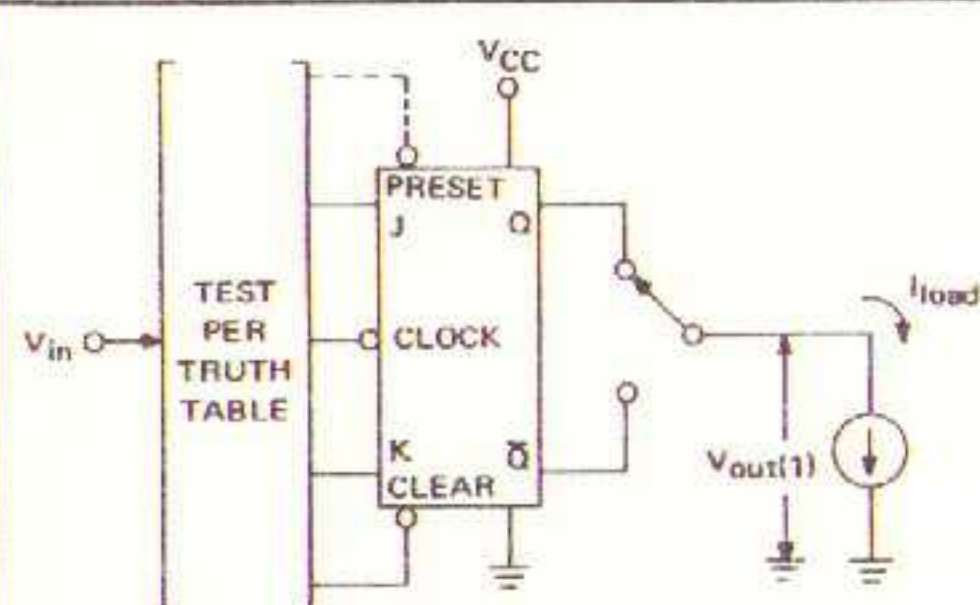
FIGURE 44

TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2



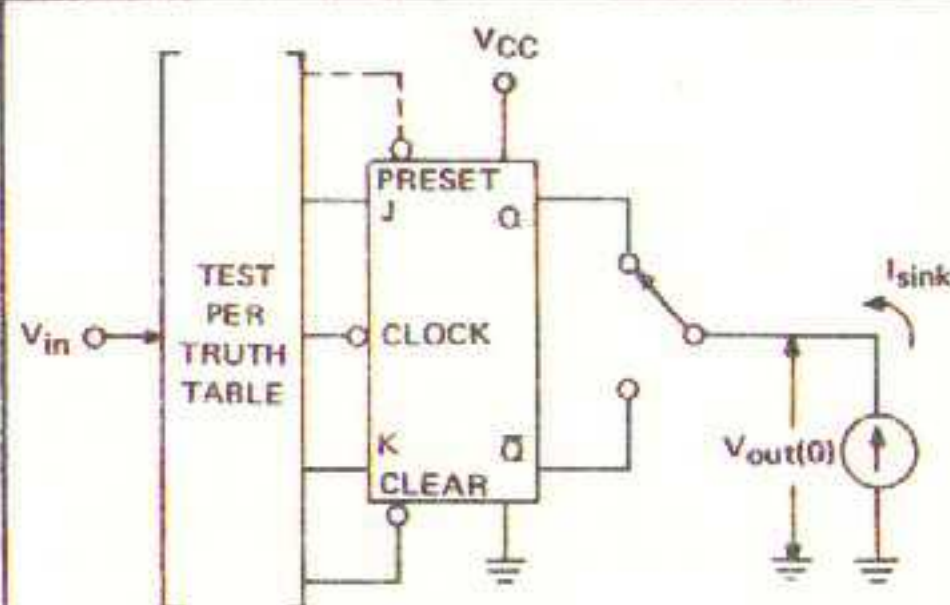
1. Each output is tested separately.

FIGURE 45



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 46



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 47

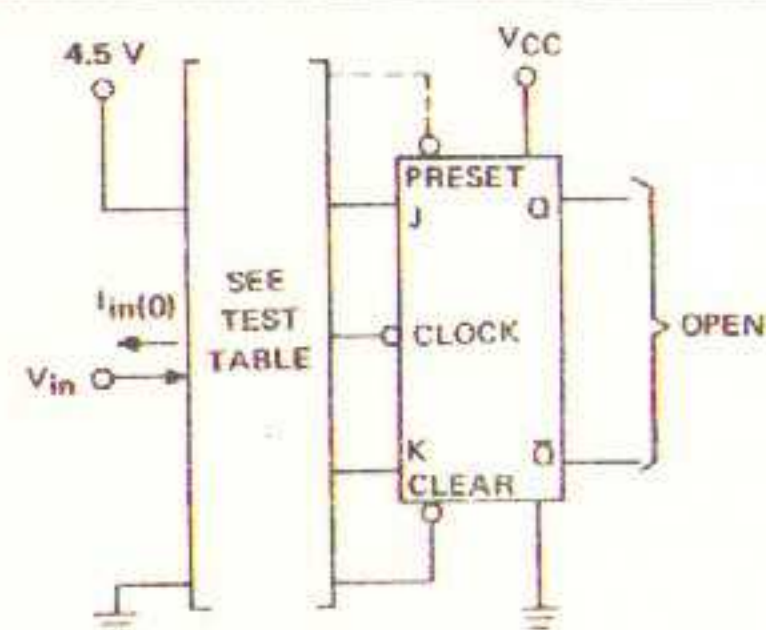


FIGURE 48

TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and $\bar{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN5476/SN7476 circuits only.

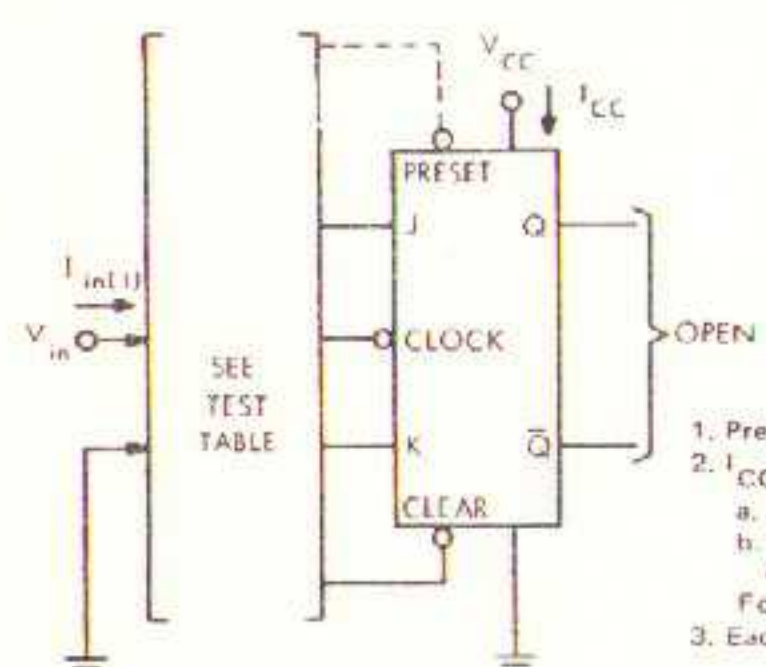
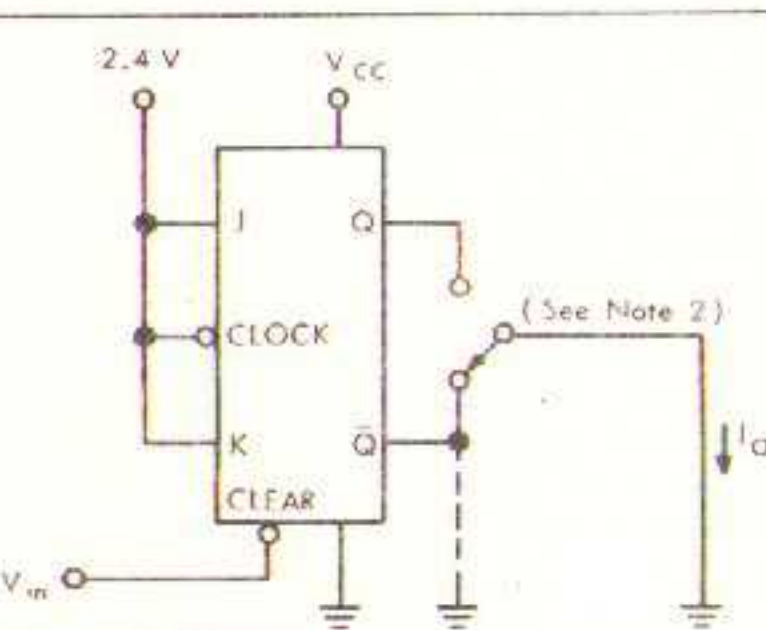


FIGURE 49

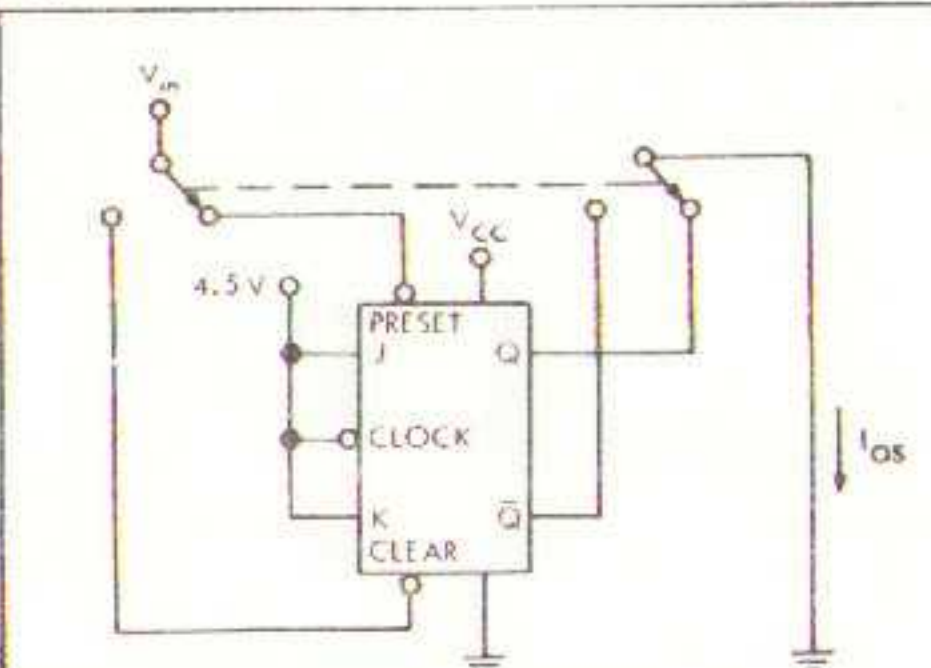
TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 1)	Clock and Preset	Clear

1. Preset is applicable for SN5476/SN7476 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
a. J = K = Clock = Clear = GND. For SN5476/SN7476: Preset = 4.5 V.
b. For SN5473/SN7473: J = Clear = 4.5 V, K = GND, and apply momentary 4.5 V, then GND to Clock.
For SN5476/SN7476: J = K = Clock = Preset = GND, and Clear = 4.5 V.
3. Each flip-flop is tested separately for $I_{in(1)}$.



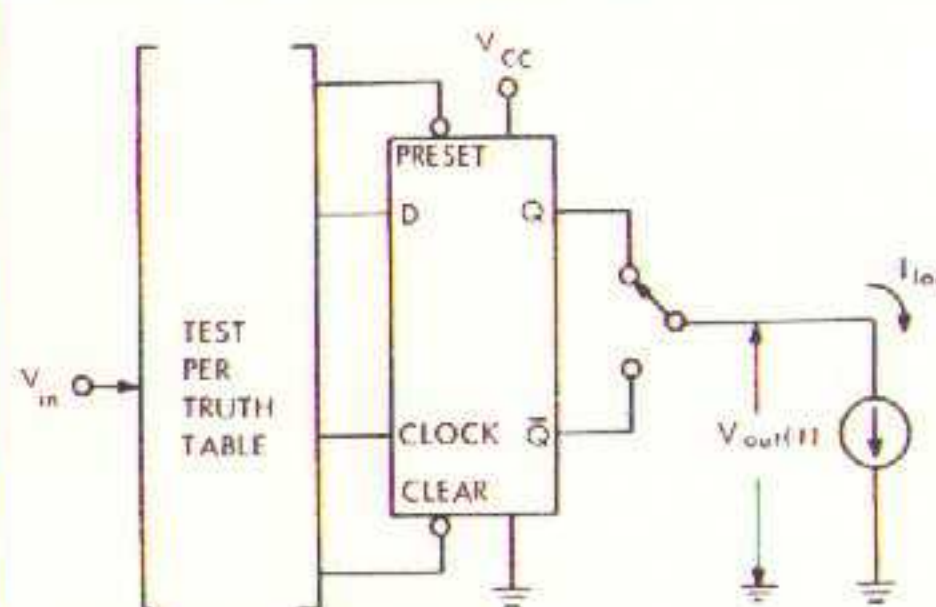
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing Q. When testing Q, apply 2.4 V to Clear, ground Q, and limit duration of test to 100 ms.

FIGURE 50



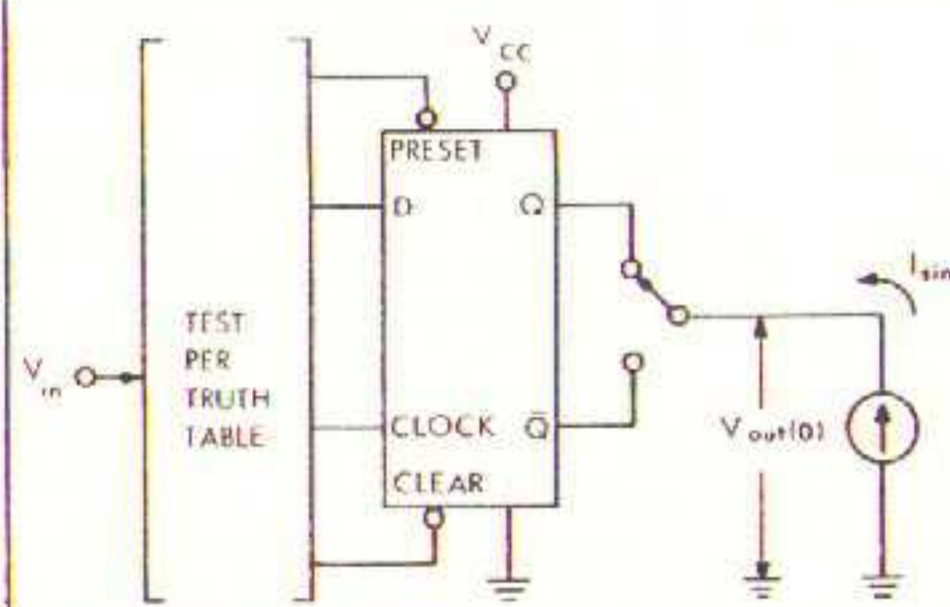
1. Each flip-flop is tested separately.

FIGURE 51



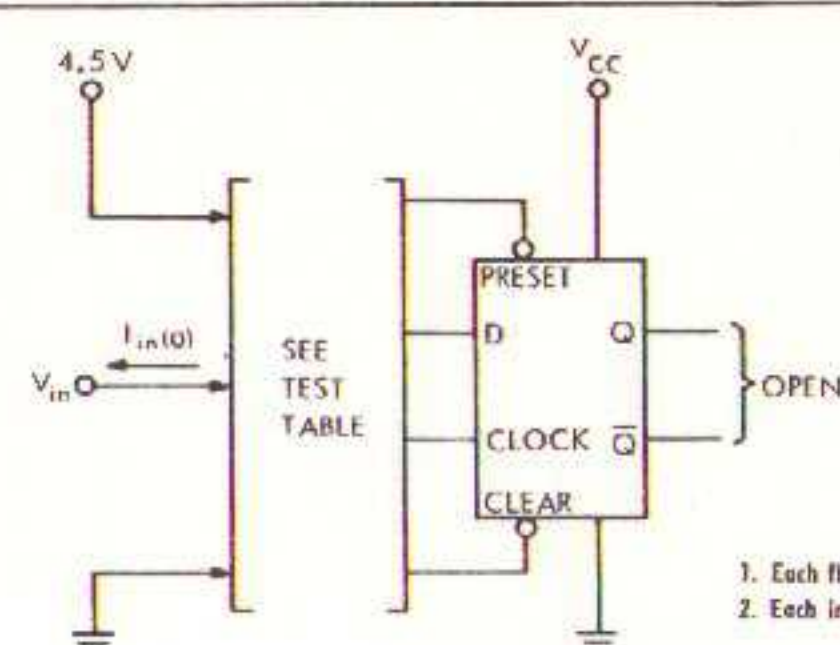
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 52



1. Each flip-flop is tested separately.
2. Each output is tested separately.

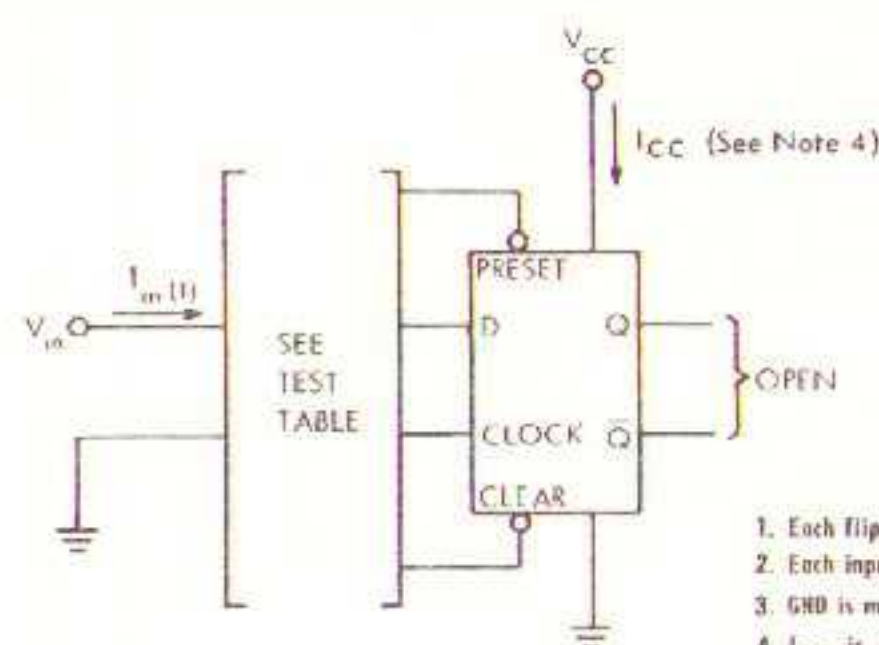
FIGURE 53



1. Each flip-flop is tested separately.
2. Each input is tested separately.

FIGURE 54

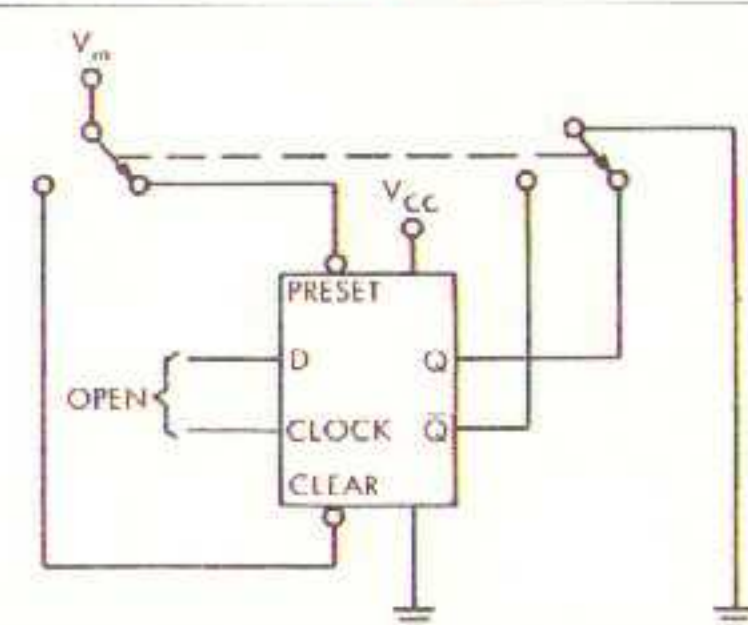
TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Apply GND
Clock	Clear and Preset	D
Preset	Clear and Clock	D
Clear	Clock and D	None
D	Clear and Clock	Preset



1. Each flip-flop is tested separately.
2. Each input is tested separately.
3. GND is momentarily applied to clock, then 4.5 V.
4. I_{CC} is measured with D, clock, and preset at GND, then with D, clock, and clear at GND.

FIGURE 55

TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Apply 4.5 V	Apply GND
Clock	None	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	D and Clock	None
D	Clock	Clear



1. Each output is tested separately.

FIGURE 56

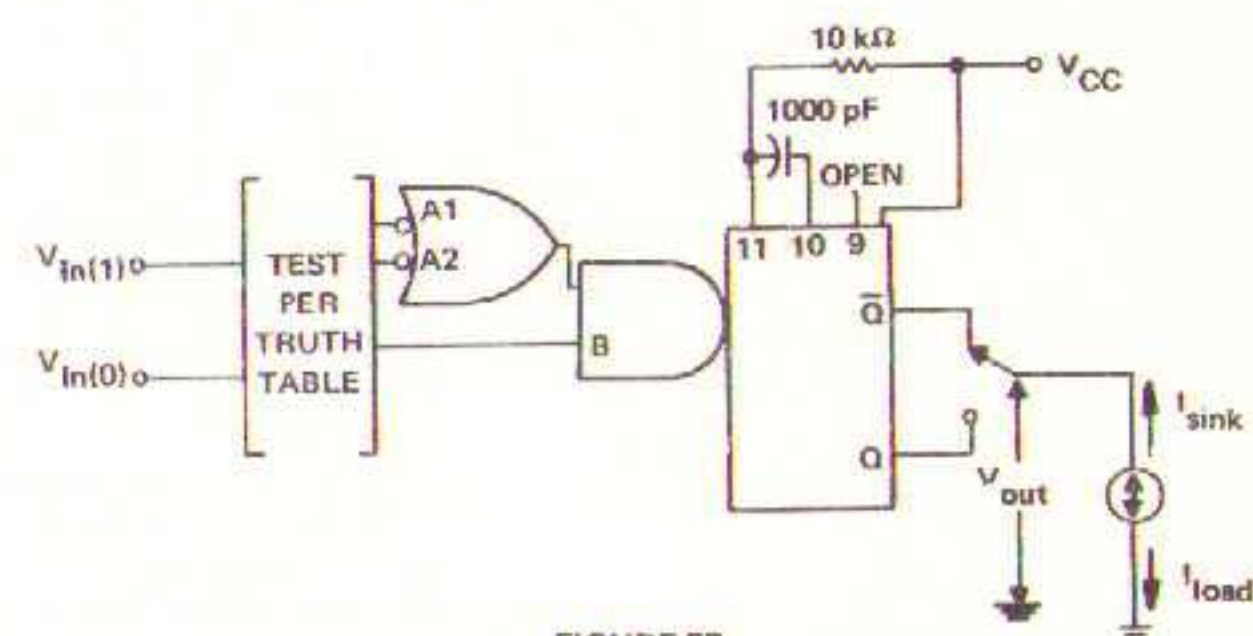
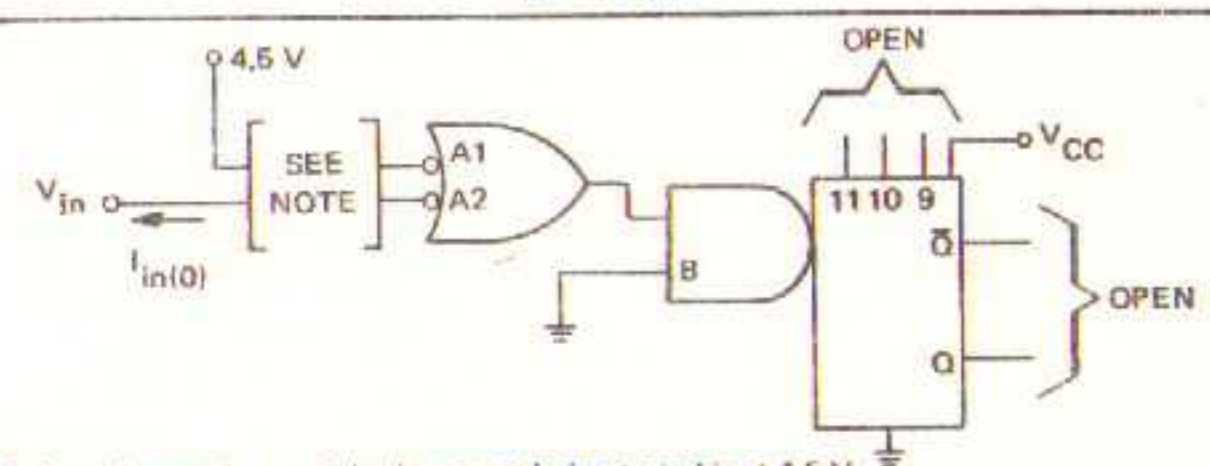


FIGURE 57



1. Each input is tested separately. Input not being tested is at 4.5 V.

FIGURE 58

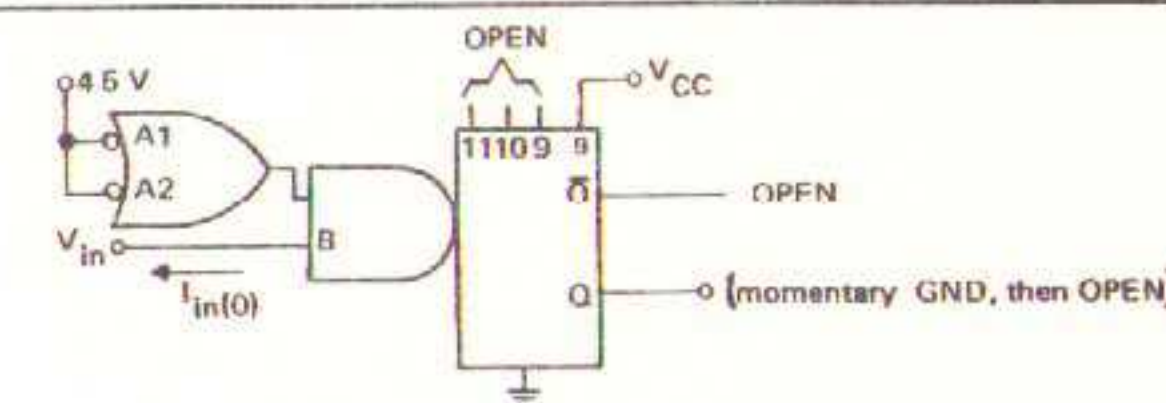
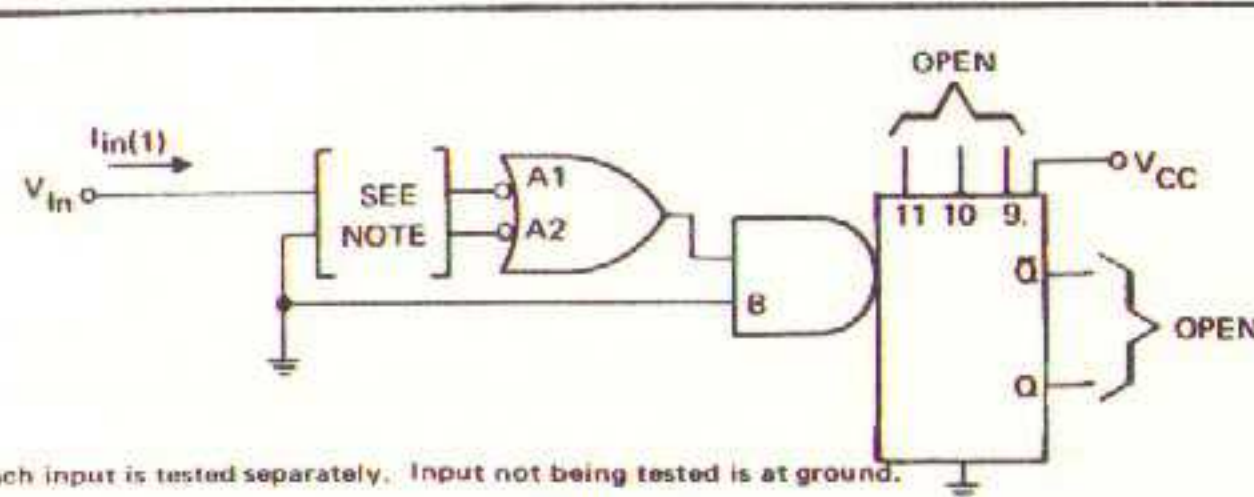


FIGURE 59



1. Each input is tested separately. Input not being tested is at ground.

FIGURE 60

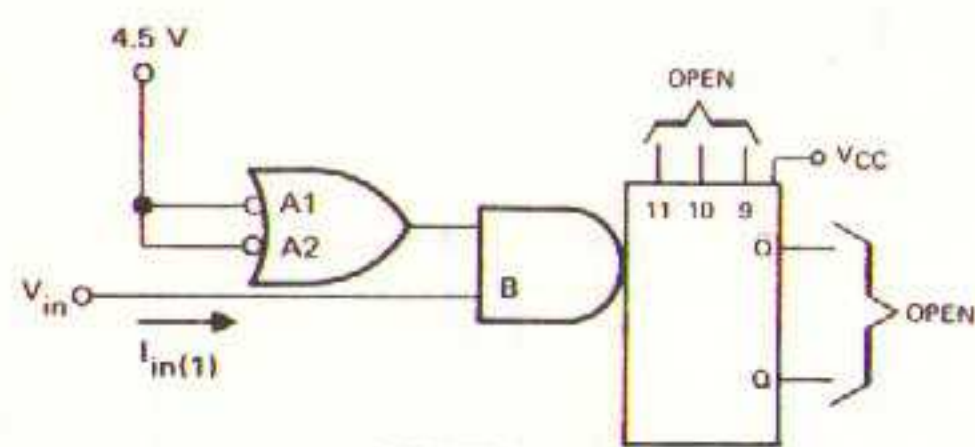


FIGURE 61

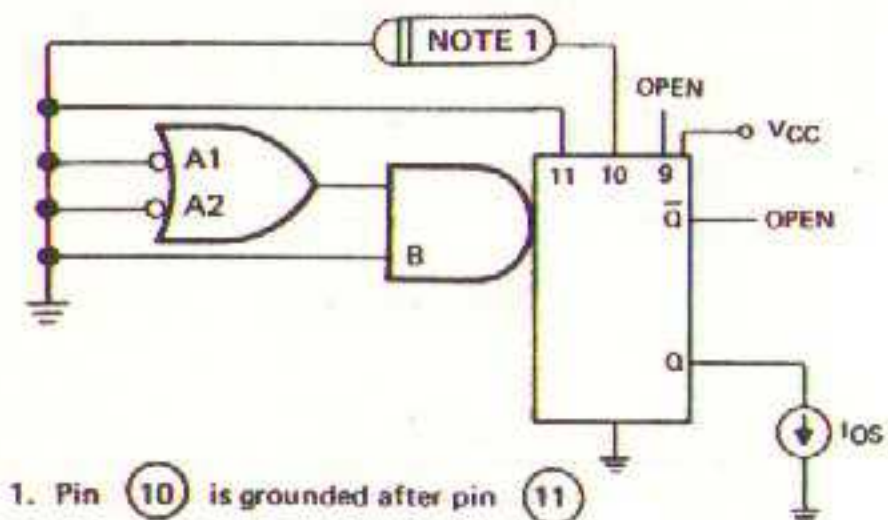


FIGURE 62

1. Pin (10) is grounded after pin (11)

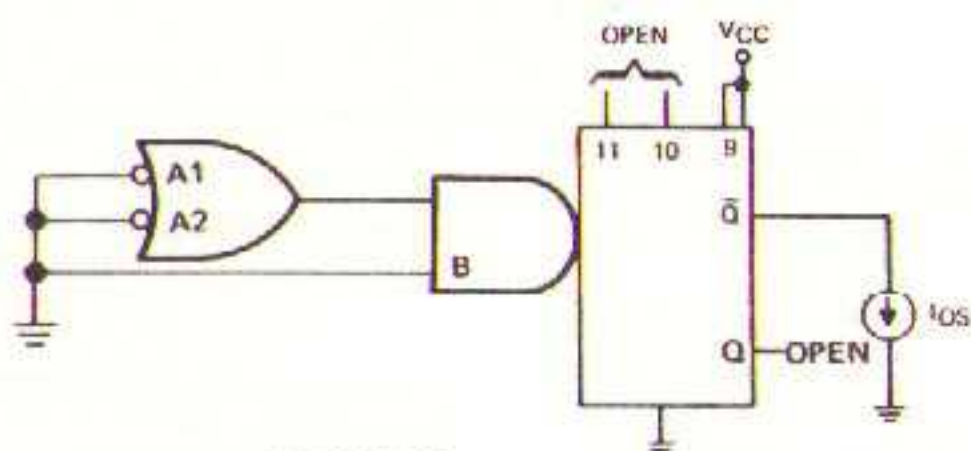


FIGURE 63

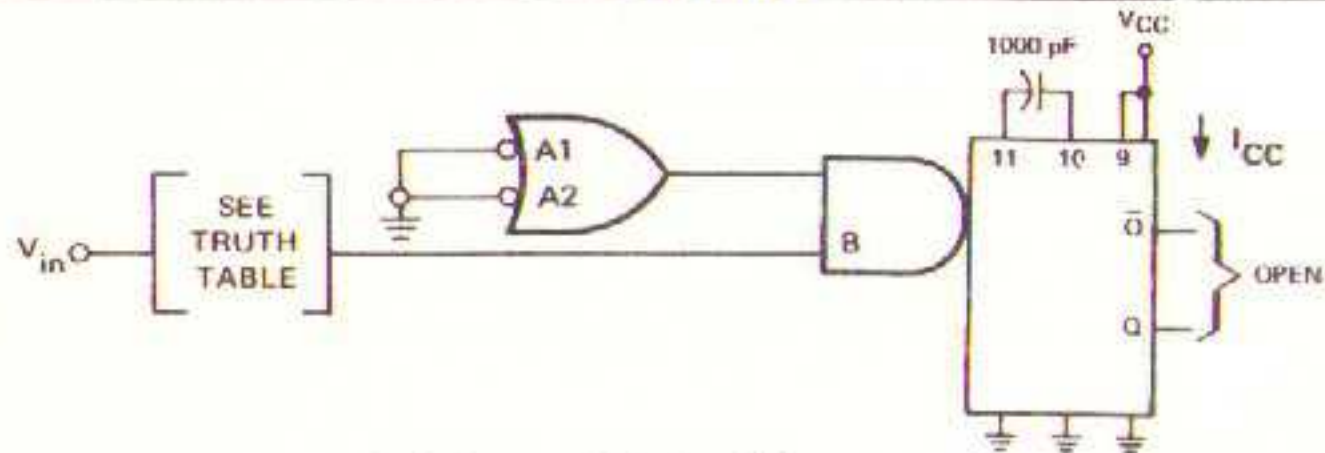
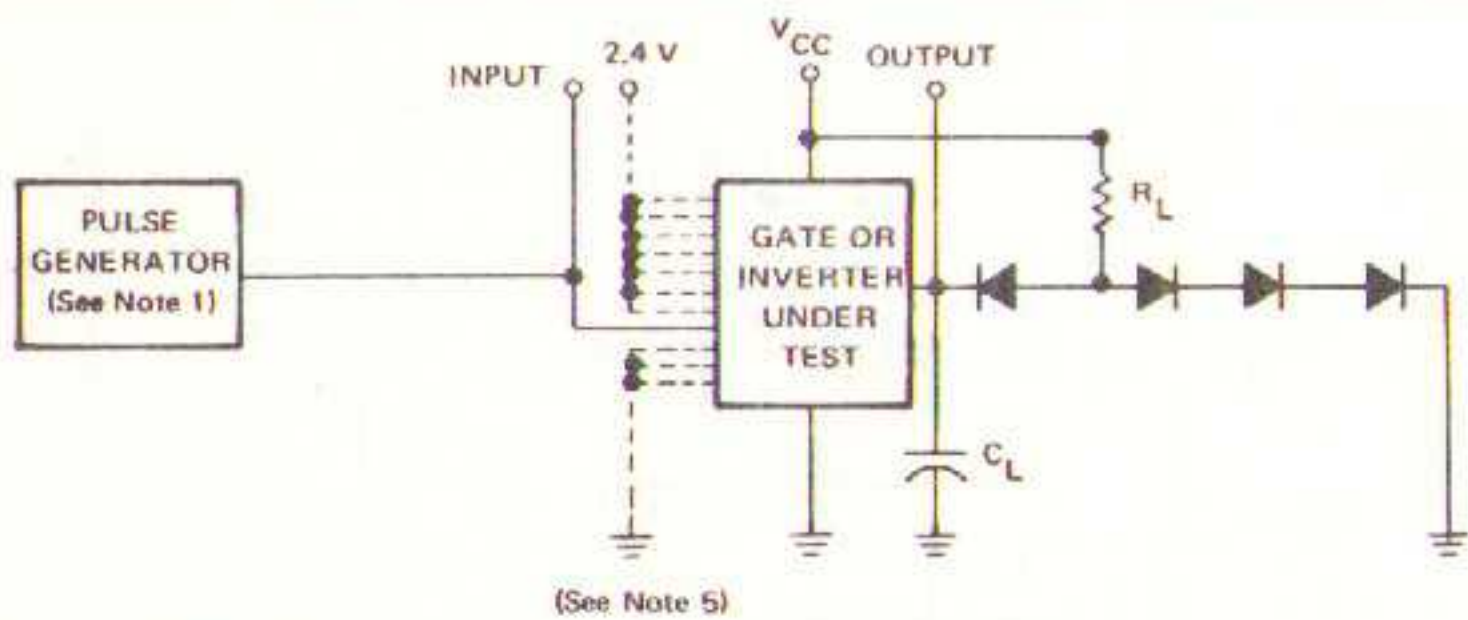
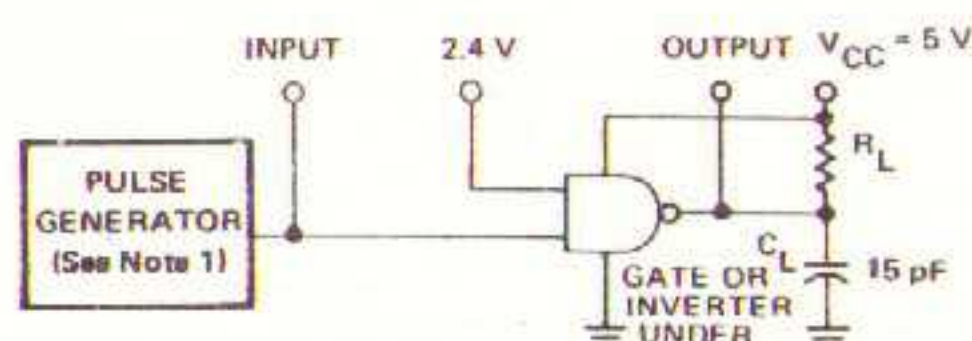


FIGURE 64

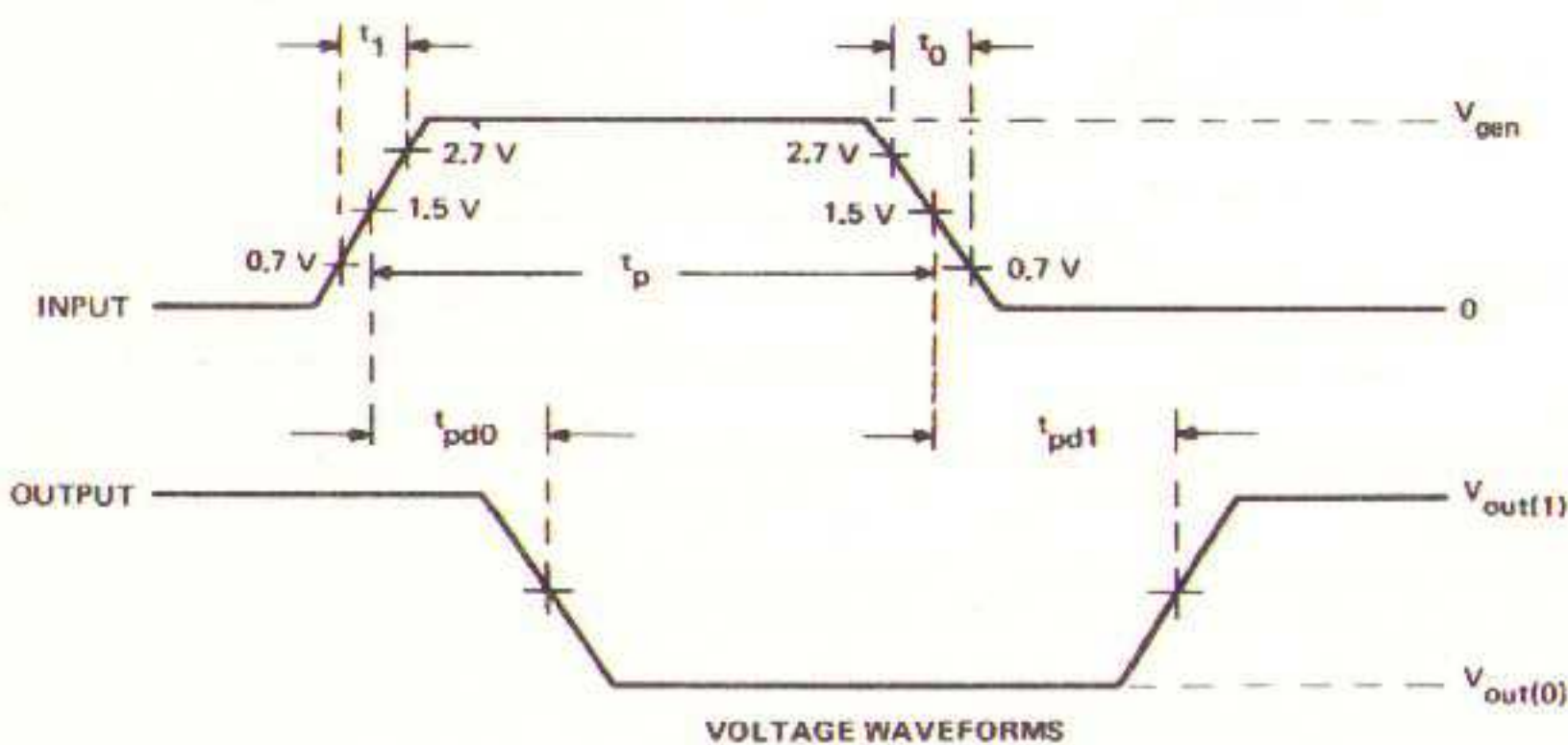
1. Quiescent and fired conditions are tested.



TEST CIRCUIT FOR SN5400, SN5402, SN5404, SN5410, SN5420, SN5430, SN5440, SN5450, SN5451, SN5453, SN5454, SN7400, SN7402, SN7404, SN7410, SN7420, SN7430, SN7440, SN7450, SN7451, SN7453, AND SN7454



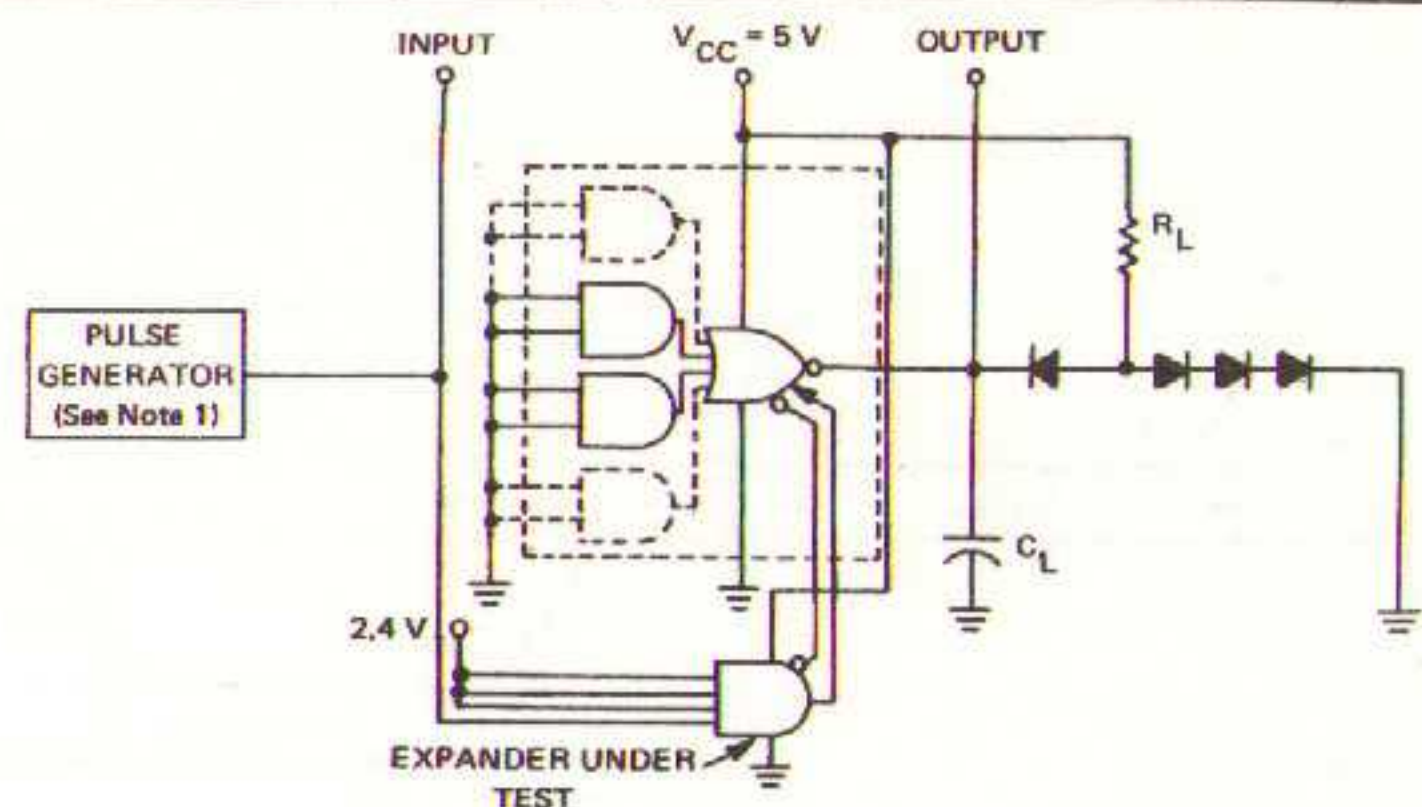
TEST CIRCUIT FOR SN5401, SN5405, SN7401, SN7405



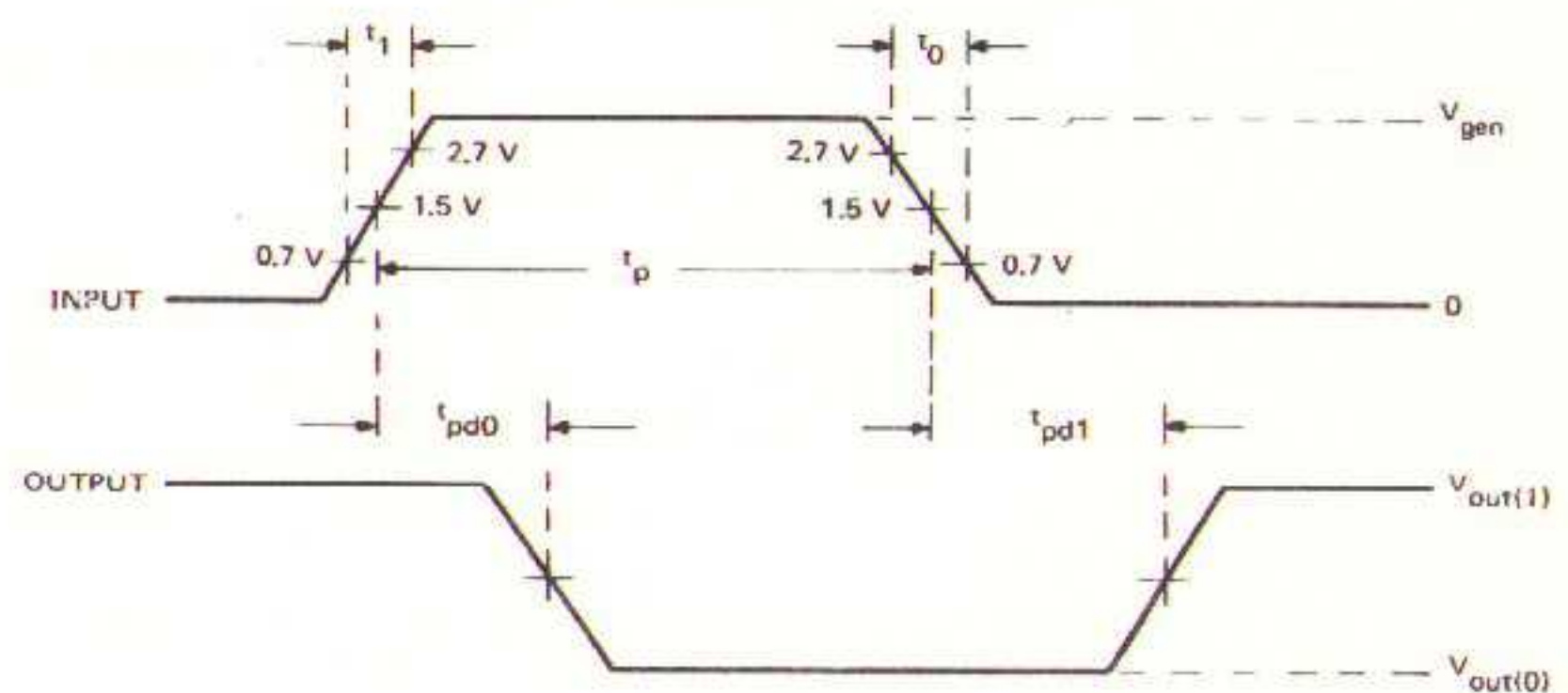
VOLTAGE WAVEFORMS

- NOTES:
1. The generator has the following characteristic: $V_{gen} = 3.5V$, $t_0 = 5ns$, $t_1 = 10ns$, $t_p = 0.5\mu s$, $PRR = 1MHz$, $Z_{out} \approx 50\Omega$.
 2. All diodes are 1N3064.
 3. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
 4. C_L includes probe and jig capacitance.
 5. When testing the SN5400/SN7400 through SN5440/SN7440 (except SN5402/SN7402) connect all unused inputs to 2.4V. When testing the SN5402/SN7402 or SN5450/SN7450 through SN5454/SN7454, apply the input pulse to one input of one AND section and 2.4V to all unused inputs of that AND section. All inputs of unused AND sections are grounded.

FIGURE 65-GATE PROPAGATION DELAY TIMES



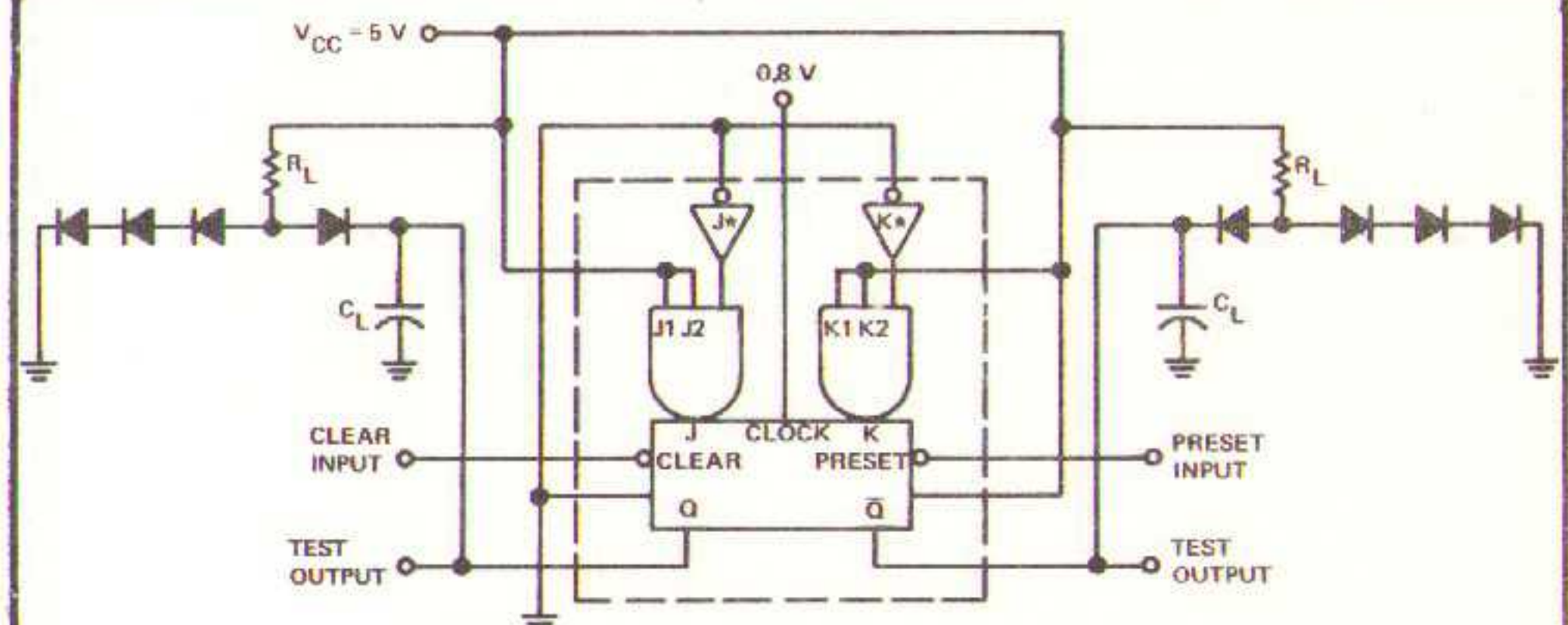
TEST CIRCUIT



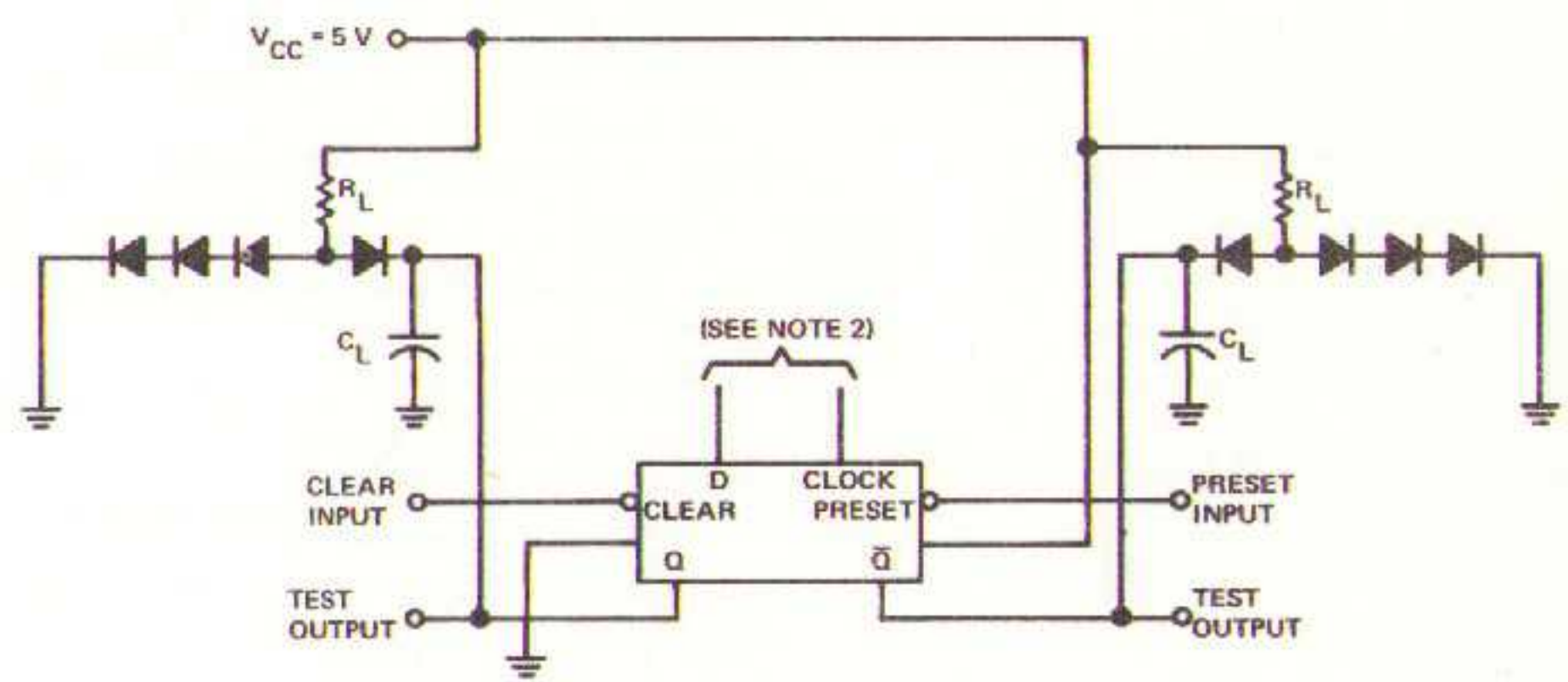
VOLTAGE WAVEFORMS

- NOTES:
1. The generator has the following characteristics: $V_{gen} = 3.5V$, $t_0 = 5ns$, $t_1 = 10ns$, $t_p = 0.5\mu s$, $PRR = 1MHz$, $Z_{out} \approx 50\Omega$.
 2. All diodes are 1N3064.
 3. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
 4. C_L includes probe and jig capacitance.

FIGURE 66-EXPANDER PROPAGATION DELAY TIMES



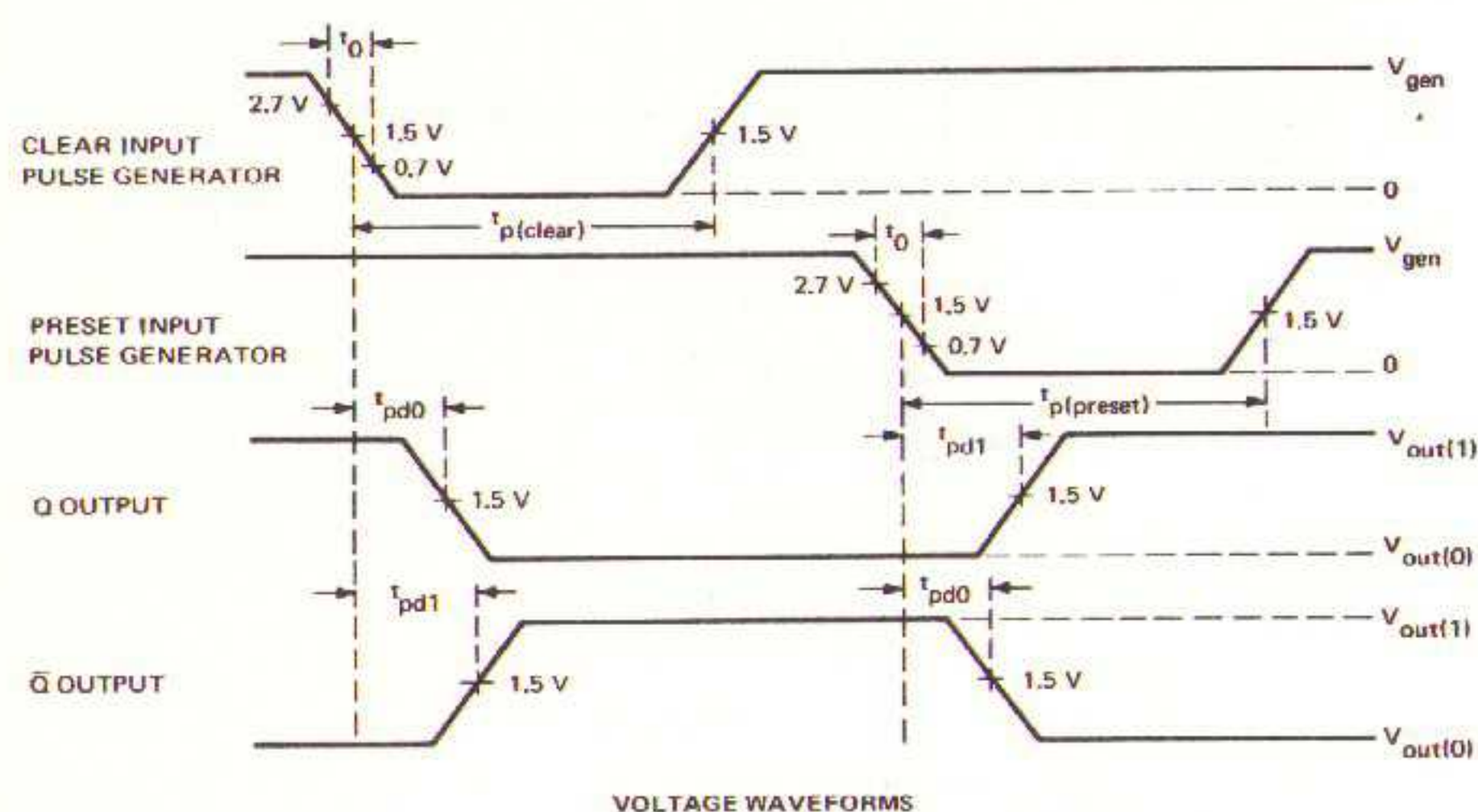
SN5470/SN7470 TEST CIRCUIT



SN5474/SN7474 TEST CIRCUIT

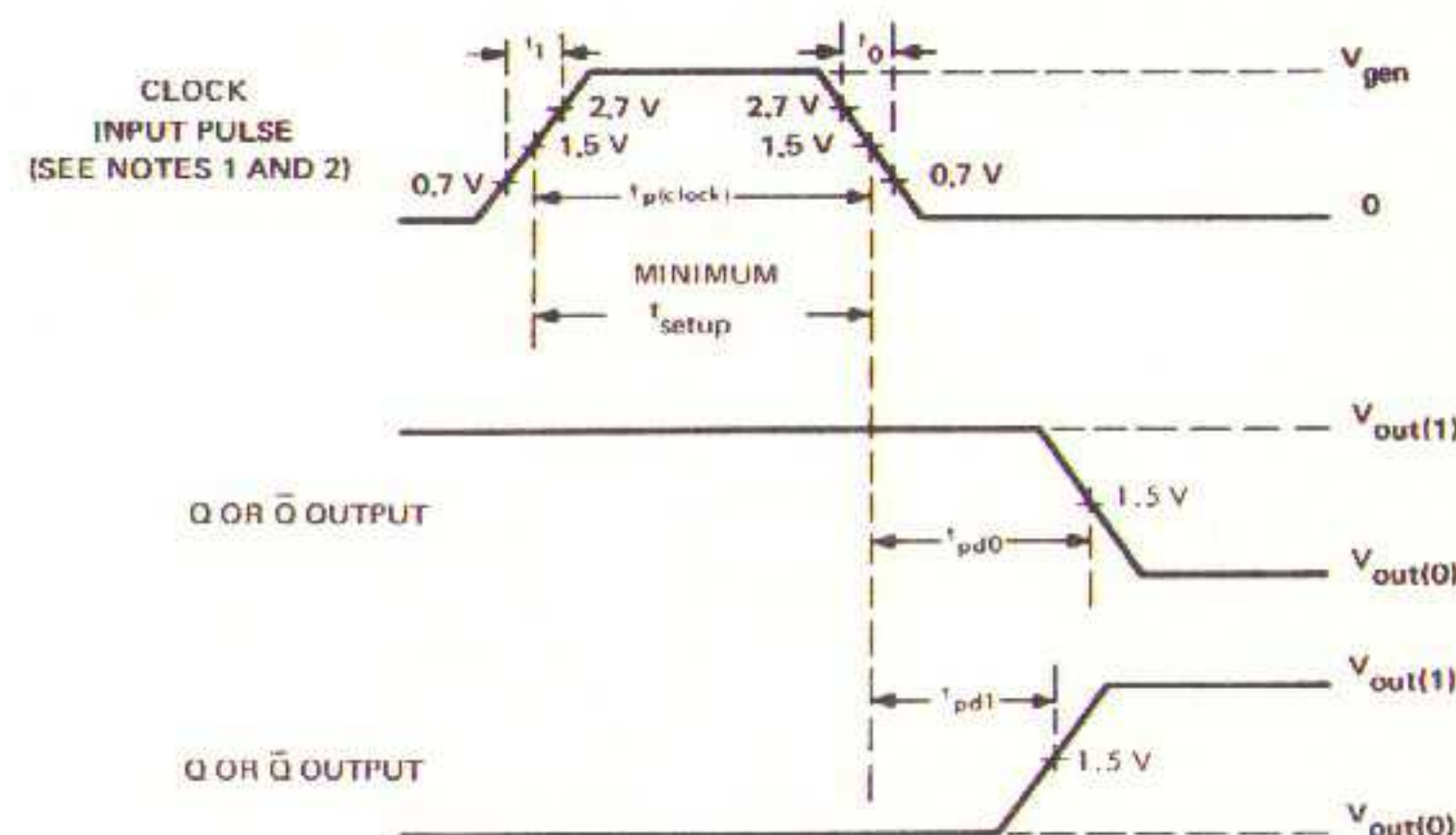
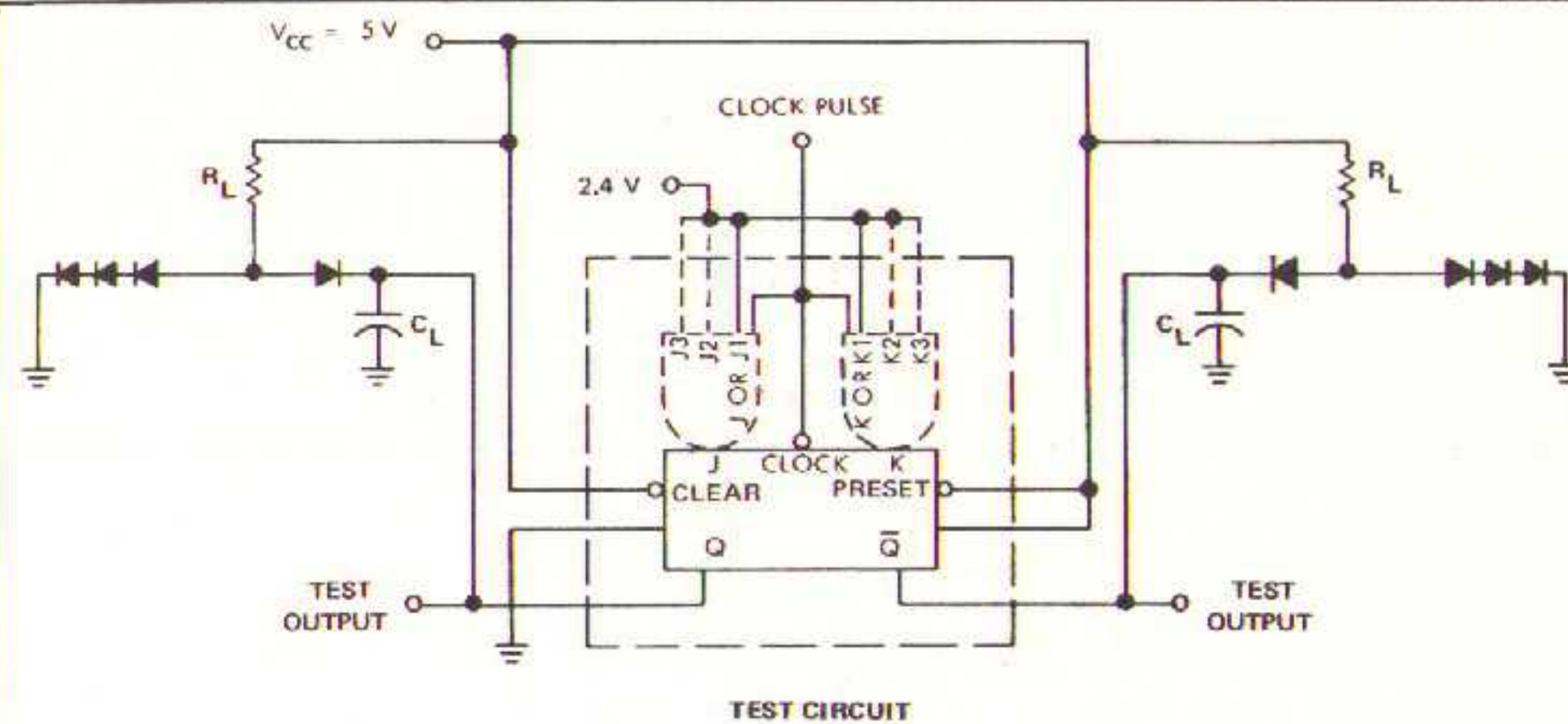
- NOTES:
1. Preset or clear function of the SN5470/SN7470 can occur only when clock input is low. Gated inputs are inhibited.
 2. Clear and preset inputs of the SN5474/SN7474 dominate regardless of the state of clock or D inputs.
 3. All diodes are 1N3064.
 4. C_L includes probe and jig capacitance.

FIGURE 67-SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 1 OF 2)



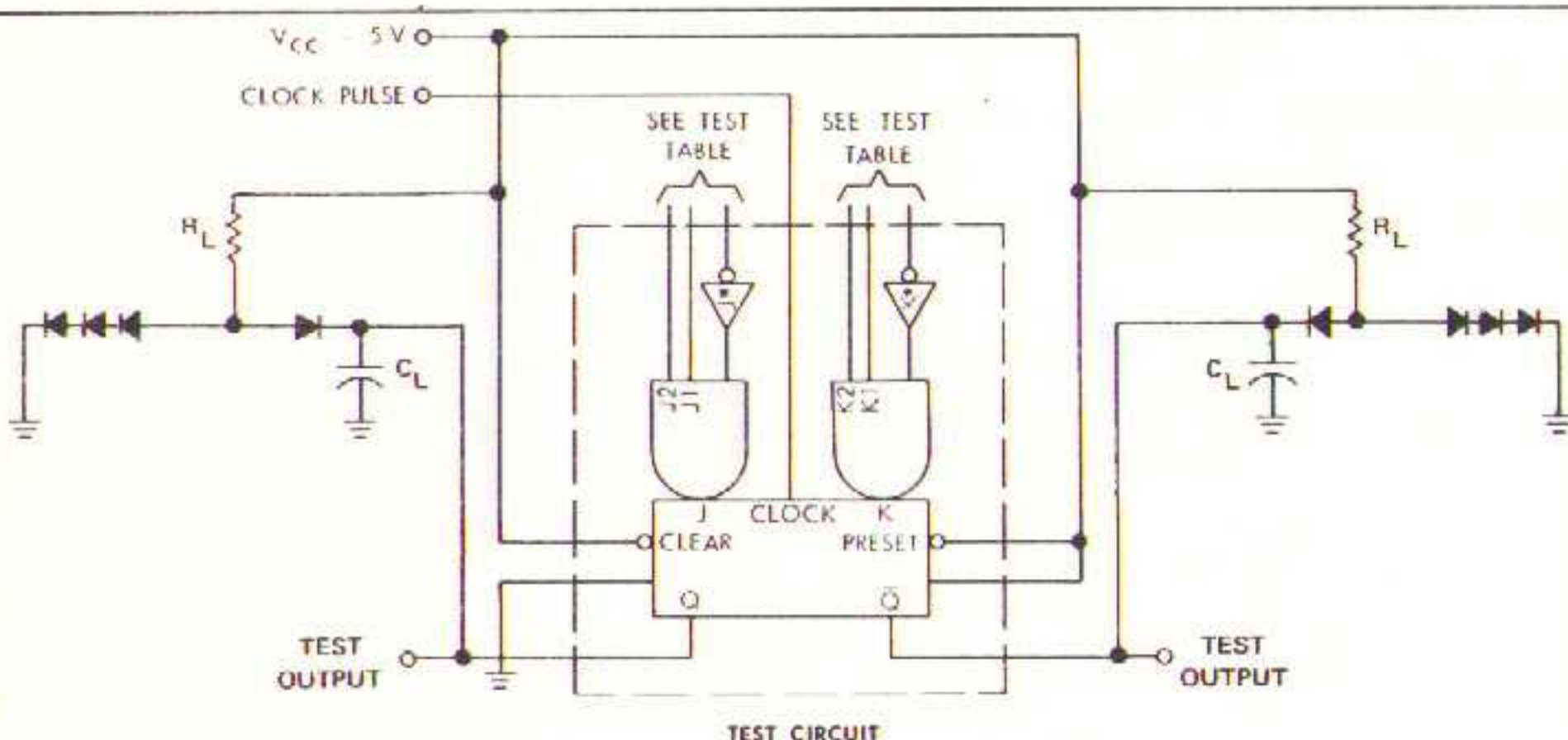
NOTE 6: Clear or preset input pulse characteristics: $V_{gen} = 3.5 \text{ V}$, $t_0 = 5 \text{ ns}$, $t_p = 25 \text{ ns}$ for the SN5470/SN7470, and $t_p = 30 \text{ ns}$ for SN5474/SN7474.

FIGURE 67—SN5470/SN7470 AND SN5474/SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)



NOTES: 1. Clock, J, and K input pulse characteristics: $V_{gen} = 3.5 \text{ V}$, $t_0 = 5 \text{ ns}$, $t_1 = 10 \text{ ns}$, $t_p = 20 \text{ ns}$, and $\text{PRR} = 1 \text{ MHz}$. When testing t_{clock} , vary PRR.
2. For the SN5472/SN7472, $J = J_1 \cdot J_2 \cdot J_3$ and $K = K_1 \cdot K_2 \cdot K_3$.
3. Gated inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN5476/SN7476, and SN54107/SN74107 Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 and SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

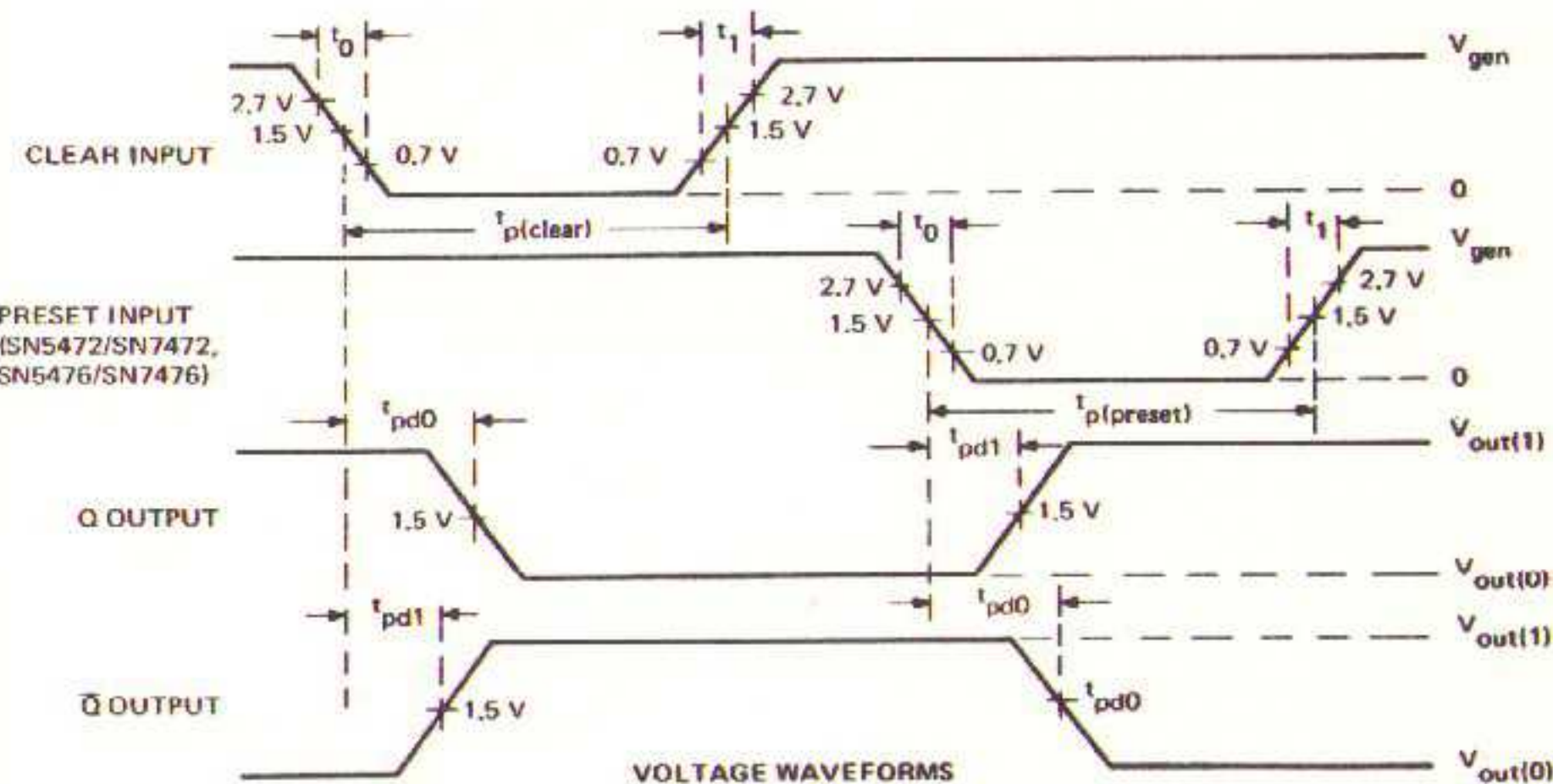
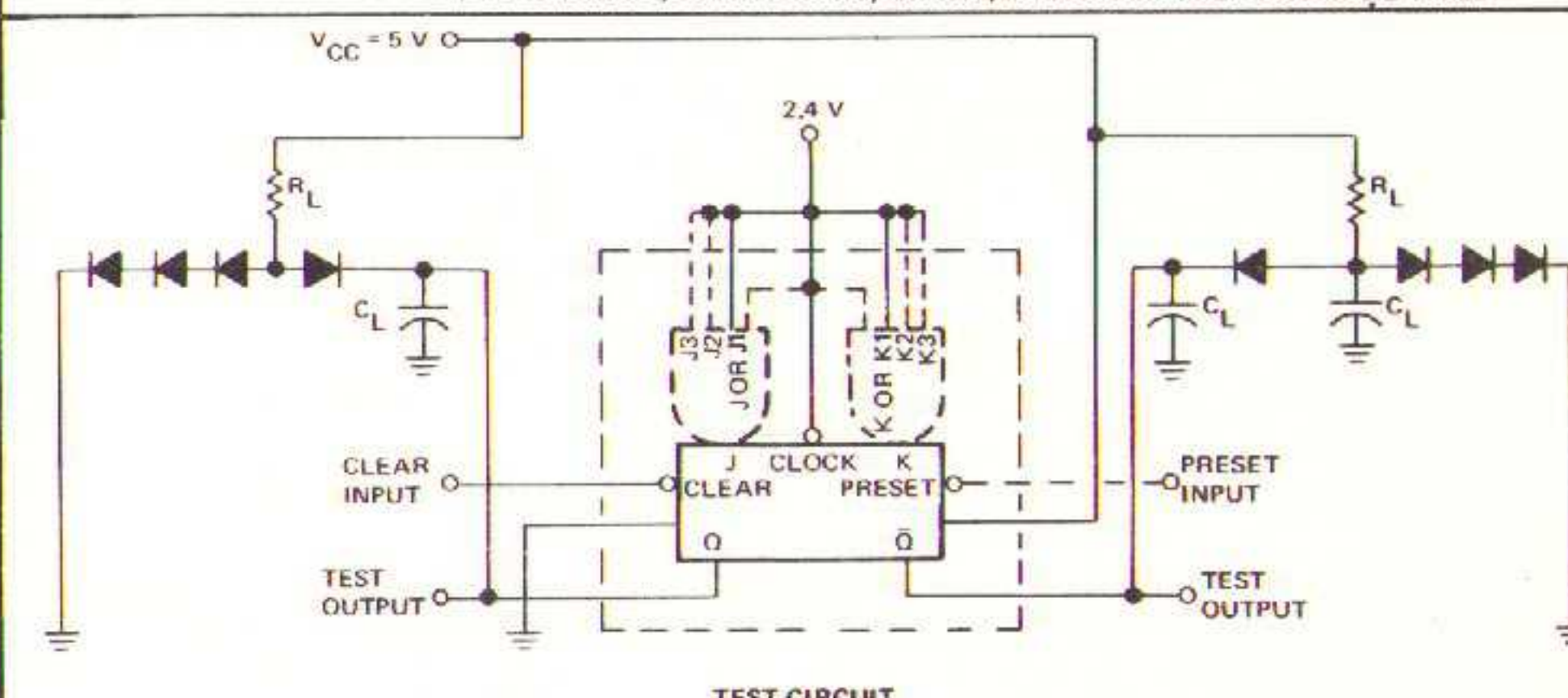
FIGURE 68—SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 FLIP-FLOP SWITCHING TIMES



TEST NO.	TEST	INPUT A	INPUT B	APPLY	GND
1	t_{setup} at J*	J*	None	J1, J2, K1, K2	K*
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J* and K*
3	t_{setup} at K*	K*	None	J1, J2, K1, K2	J*
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J* and K*

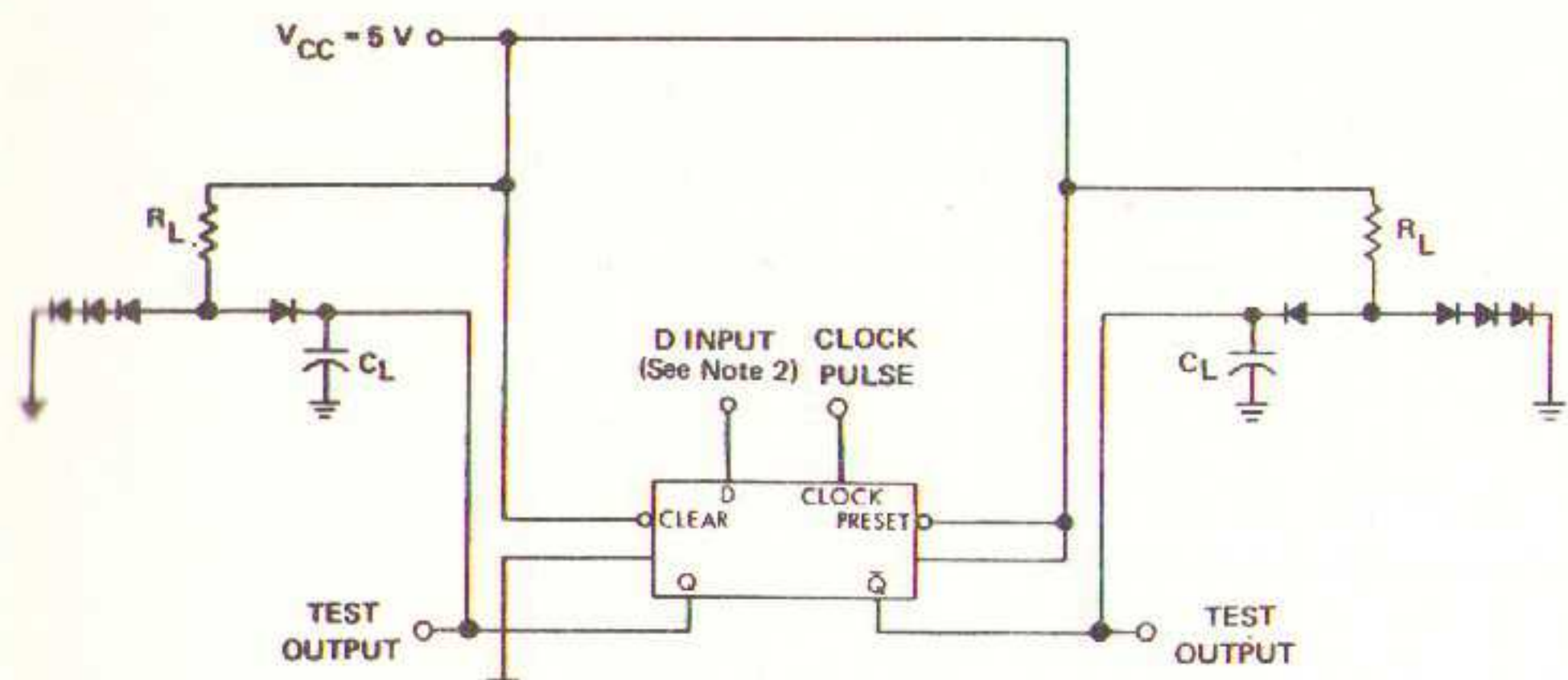
NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold} .
2. Clock frequency, t_{pd1} , and t_{pd0} (from clock to output) are measured in the toggle mode. Hold $J = K = \text{Logical 1}$ per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics: $V_{gen} = 3.5 \text{ V}$, $t_1 = 10 \text{ ns}$, $t_p = 20 \text{ ns}$, and $\text{PRR} = 1 \text{ MHz}$. When testing t_{clock} , vary PRR.
4. Input pulse characteristics: $V_{gen} = 3.5 \text{ V}$, $t_0 = 5 \text{ ns}$.
5. All diodes are 1N3064.
6. C_L includes probe and jig capacitance.

FIGURE 68—SN5470/SN7470 FLIP-FLOP SWITCHING TIMES

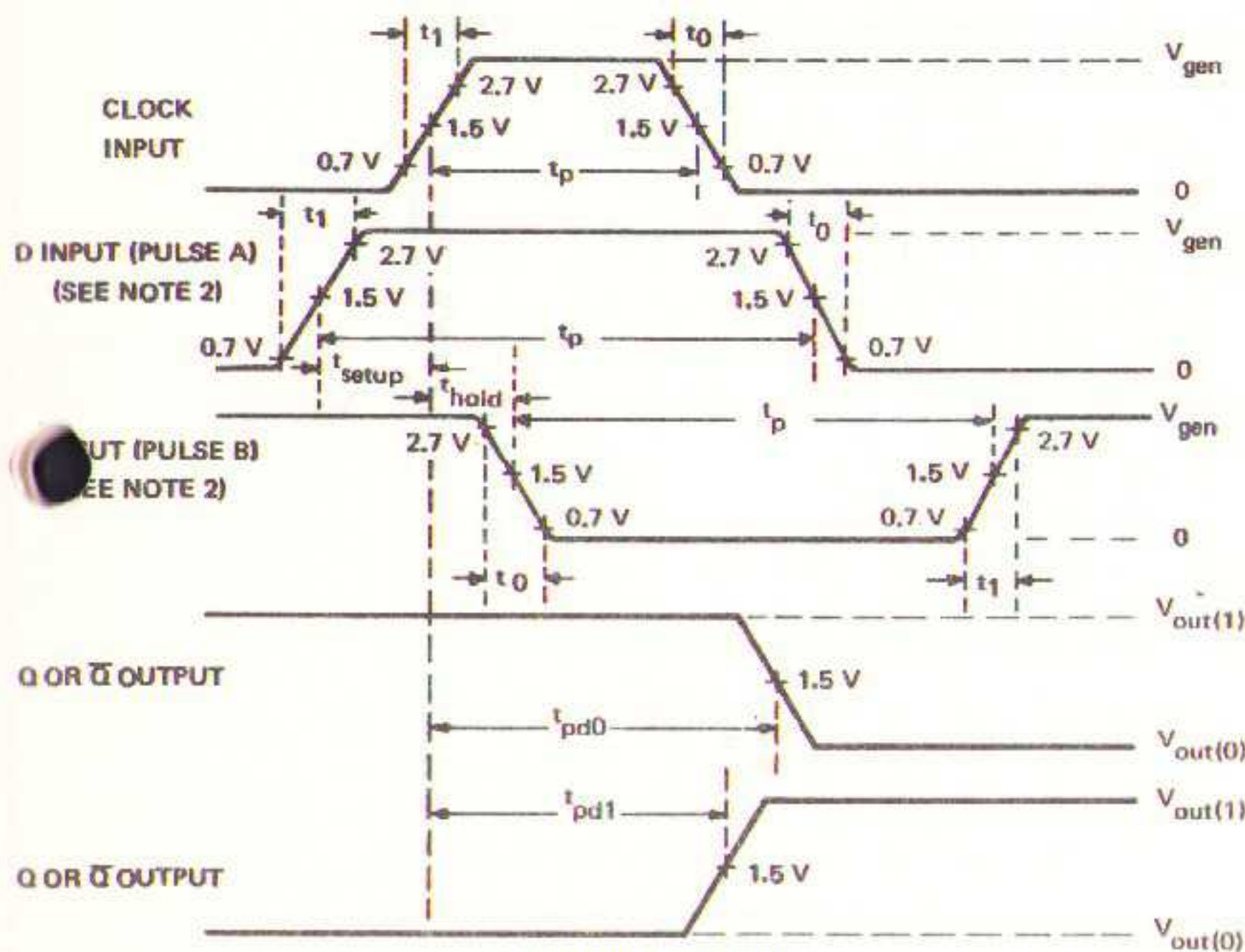


NOTES: 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: $V_{CC} = 3.5 \text{ V}$, $t_0 = 5 \text{ ns}$, $t_1 = 10 \text{ ns}$, $t_p(\text{clear}) = t_p(\text{preset}) = 25 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, and $Z_{out} \approx 50 \Omega$.
3. Gated inputs (shown with dotted lines) are for the SN5472/SN7472 only. The SN5473/SN7473, SN5476/SN7476, and SN54107/SN74107 Dual Flip-Flops have direct J and K inputs, and preset is not available on the SN5473/SN7473 or SN54107/SN74107.
4. All diodes are 1N3064.
5. C_L includes probe and jig capacitance.

FIGURE 70—SN5472/SN7472, SN5473/SN7473, SN5476/SN7476, SN54107/SN74107 PRESET/CLEAR PROPAGATION DELAY TIMES



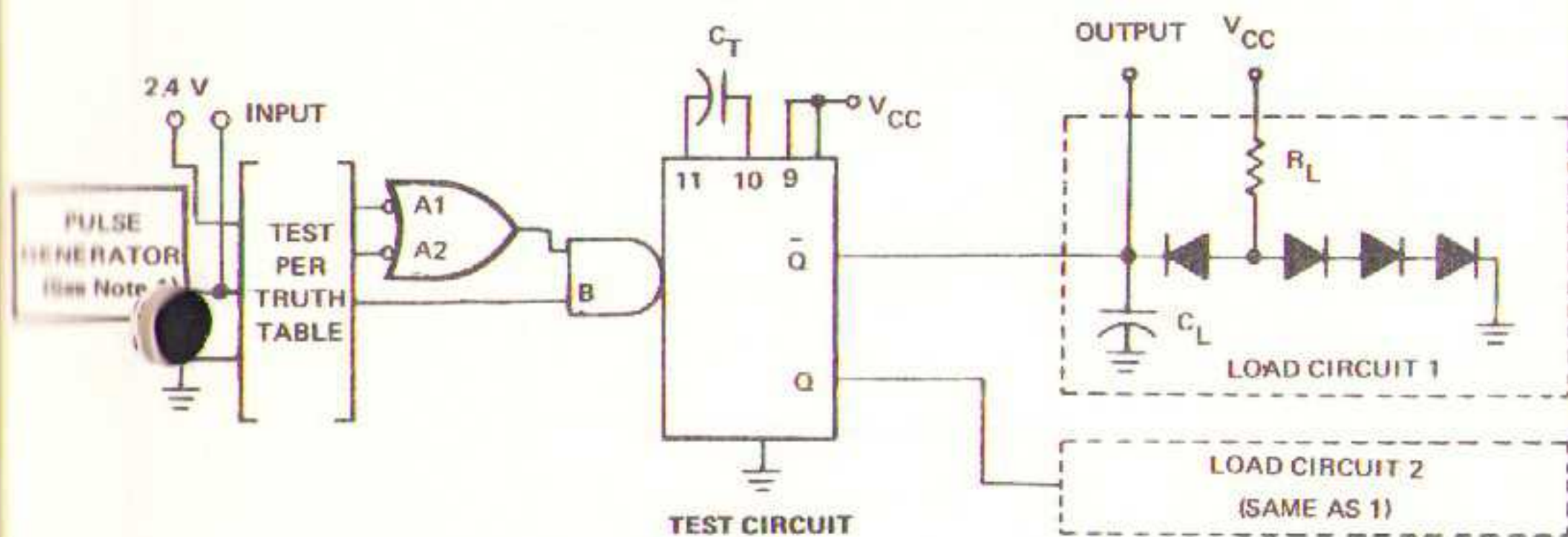
TEST CIRCUIT



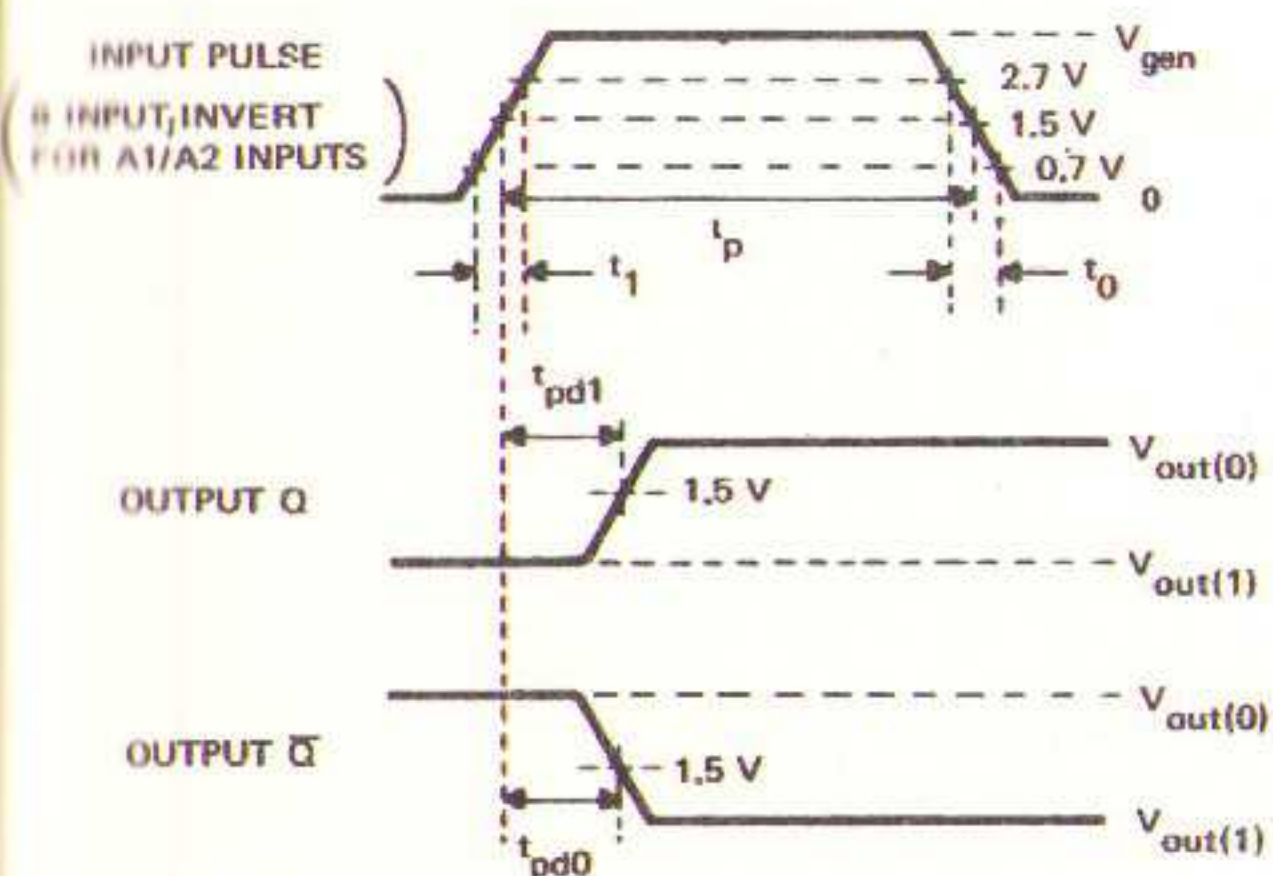
VOLTAGE WAVEFORMS

1. Clock input pulse has the following characteristics: $V_{gen} = 3.5\text{ V}$, $t_0 = 5\text{ ns}$, $t_1 = 10\text{ ns}$, $t_2 = 30\text{ ns}$, and $PRR = 1\text{ MHz}$. When testing t_{pd0} vary PRR .
2. D input (pulse A) has the following characteristics: $V_{gen} = 3.5\text{ V}$, $t_0 = 5\text{ ns}$, $t_1 = 10\text{ ns}$, $t_{setup} = 20\text{ ns}$, $t_p = 60\text{ ns}$, and PRR is 50% of the clock PRR . D input (pulse B) has the following characteristics: $V_{gen} = 3.5\text{ V}$, $t_0 = 5\text{ ns}$, $t_1 = 10\text{ ns}$, $t_{hold} = 5\text{ ns}$, $t_p = 60\text{ ns}$, and PRR is 50% of the clock PRR .
3. All diodes are 1N3064.
4. C_L includes probe and jig capacitance.

FIGURE 71—SN5474/SN7474 FLIP-FLOP SWITCHING TIMES



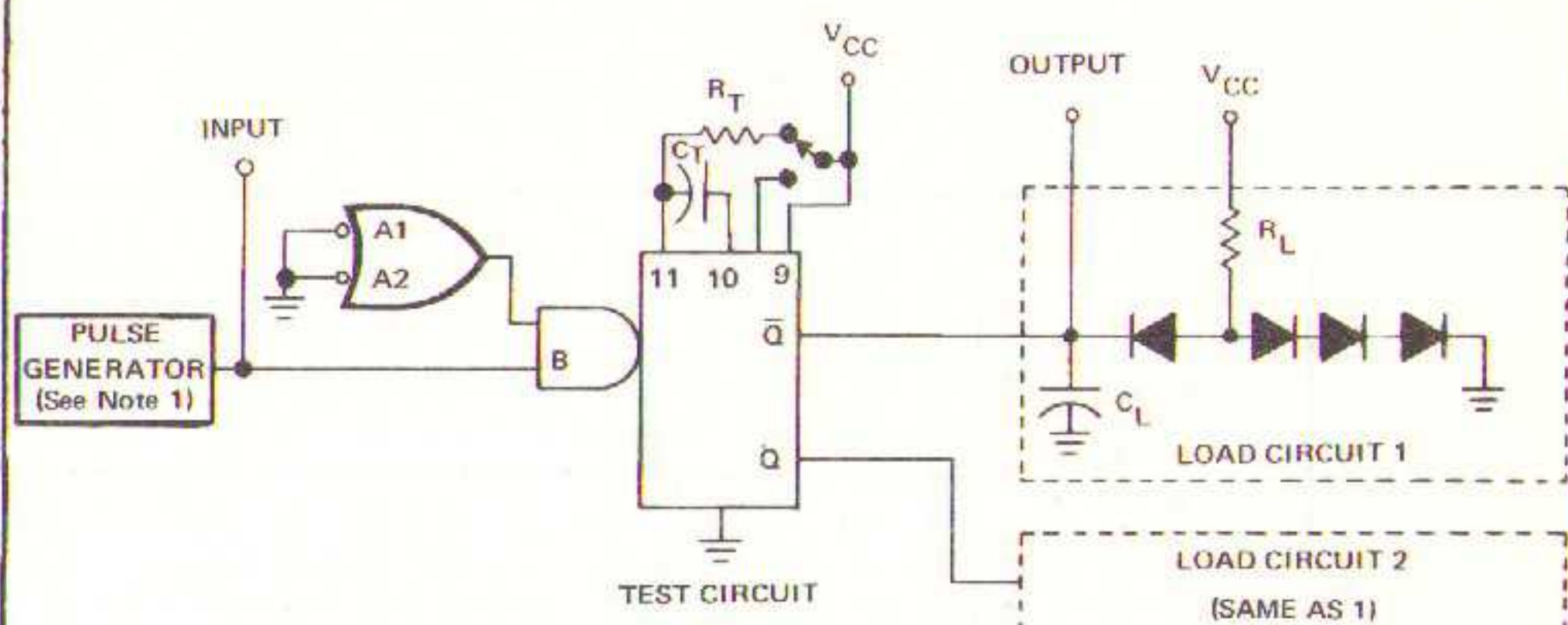
TEST CIRCUIT



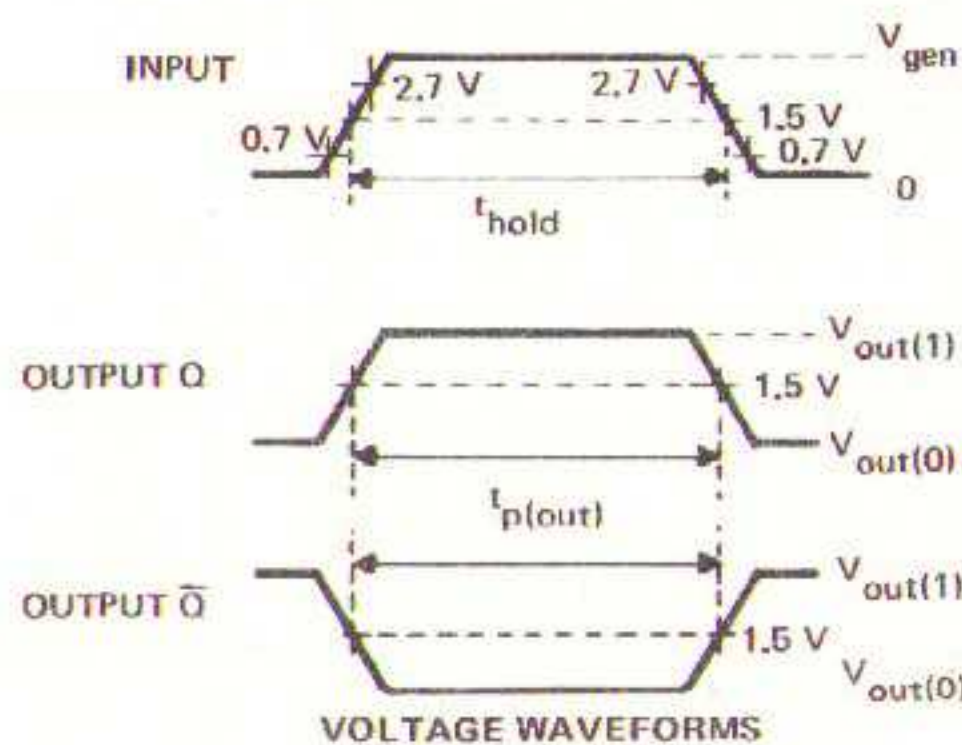
VOLTAGE WAVEFORMS

1. The pulse generator has the following characteristics: $V_{gen} = 3.5\text{ V}$, $t_0 = 5\text{ ns}$, $t_1 = 10\text{ ns}$, $t_p \geq 50\text{ ns}$, $PRR = 1\text{ MHz}$, and $Z_{out} \approx 50\text{ }\Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

FIGURE 72—SN54121/SN74121 SWITCHING TIMES



TEST CIRCUIT

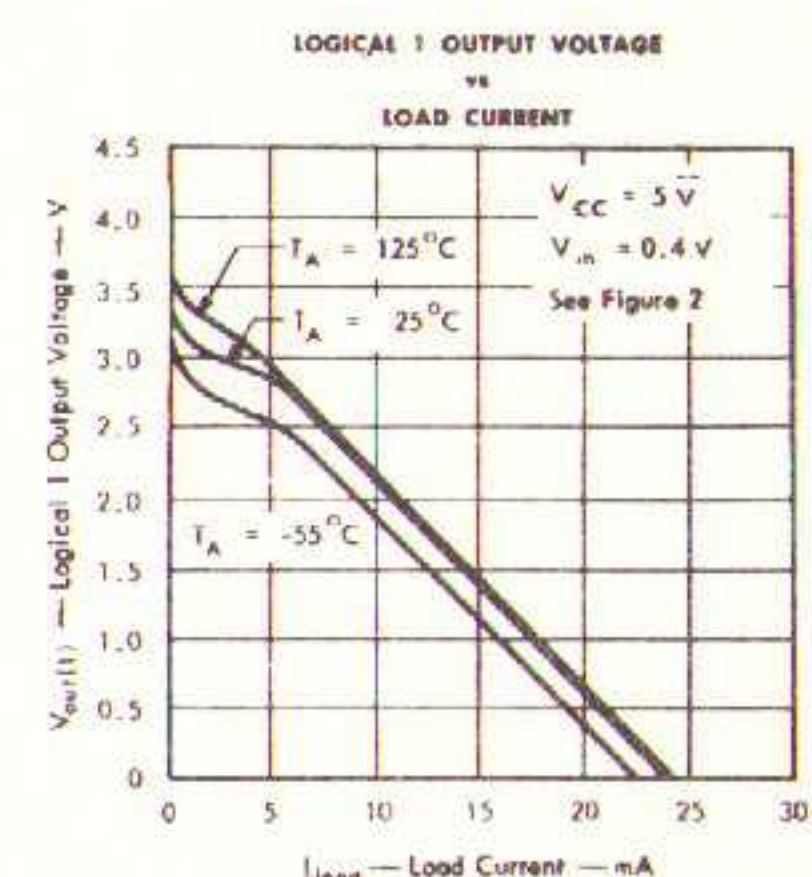
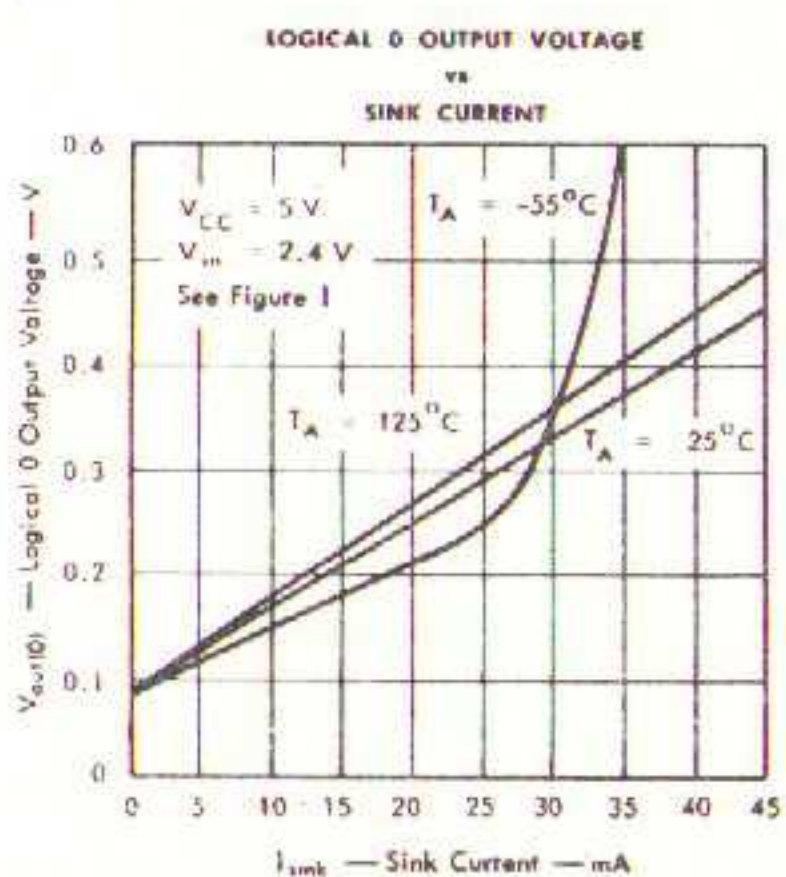
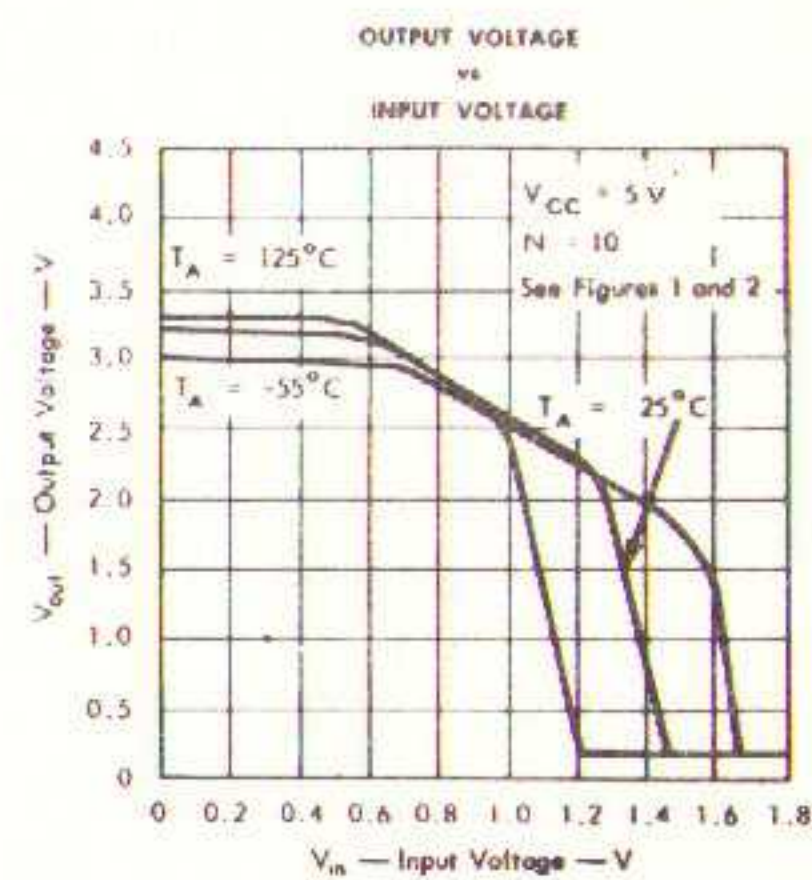
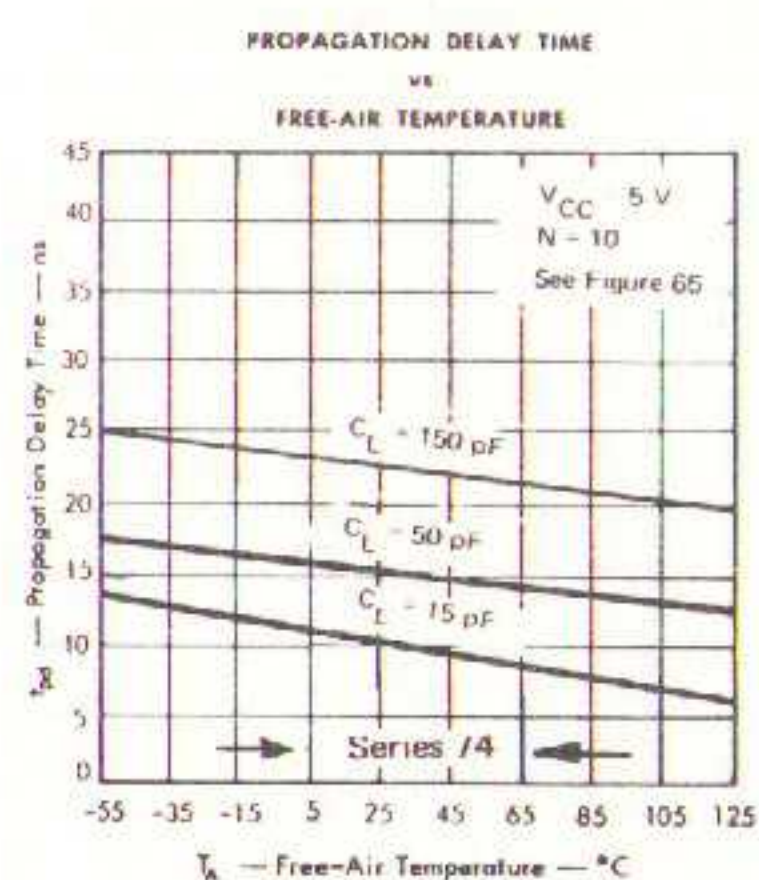
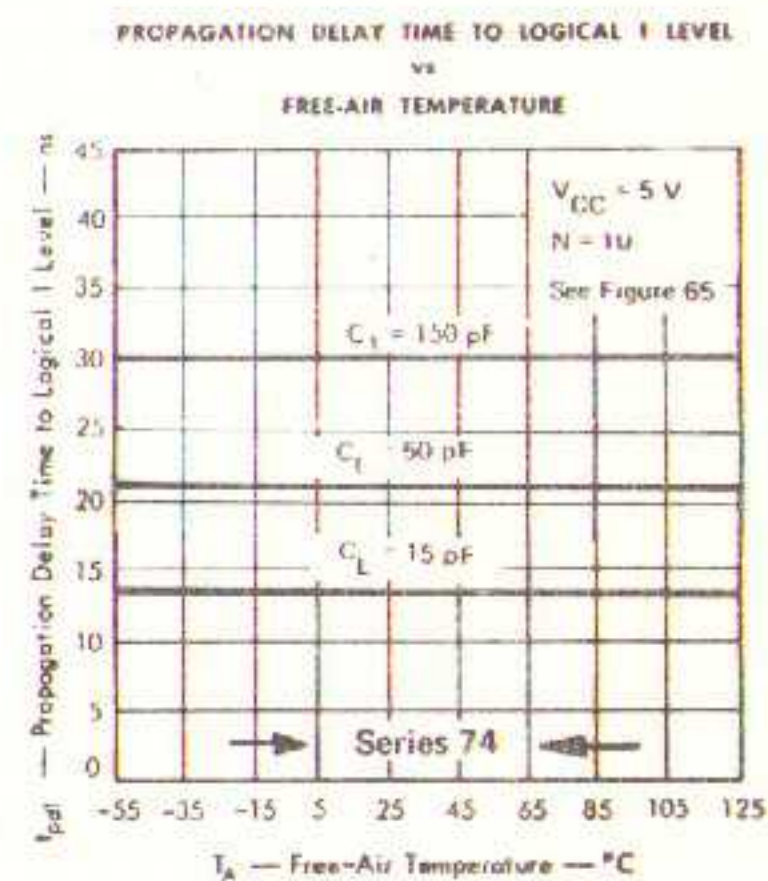
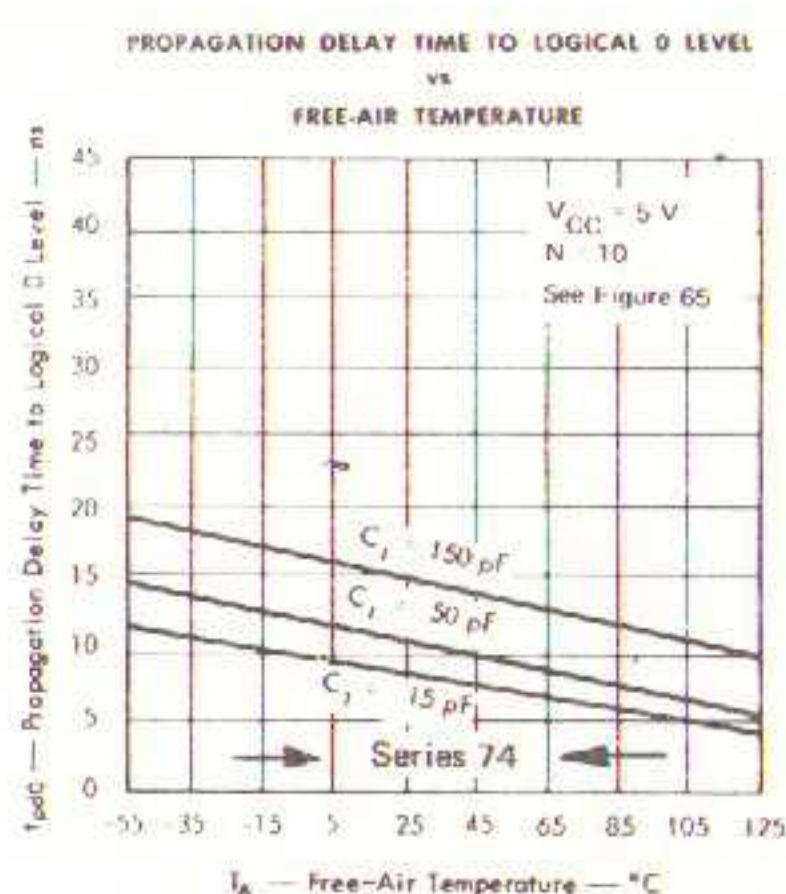


VOLTAGE WAVEFORMS

1. The pulse generator has the following characteristics: $V_{gen} = 3.5\text{ V}$, $t_0 = 5\text{ ns}$, $t_1 = 10\text{ ns}$, $t_p = 50\text{ ns}$, $PRR = 1\text{ MHz}$, and $Z_{out} \approx 50\text{ }\Omega$.
2. All diodes are 1N3064.
3. C_L includes probe and jig capacitance.

FIGURE 73— t_{pd0} (internal/minimum), t_{hold}

TYPICAL CHARACTERISTICS



O V E R Z I C H T U I T W I S S E L B A R E T T L G E Ï N T E G R E E R D E S C H A K E L I N G E N

Onderstaande typen geïntegreerde schakelingen zijn volkomen uitwisselbaar. Wij wijzen er wel op, dat bij verschillende fabrikanten kleine verschillen in de technische gegevens voorkomen. Veelal hebben deze betrekkelijk weinig invloed op Uw ontwerp. Tevens wijzen wij erop, dat de meeste fabrikanten hun reeks nog aan het uitbreiden zijn, waardoor deze lijst niet als volledig kan worden beschouwd.

AEG	AMPEREX	FAIRCHILD	FERRANTI	ITT	MOTOROLA	NSC	PHILIPS	SESCOSEM	SIEMENS	SIGNETICS	SPRAGUE	TI	TRANSITRON
FLH101	FJH131	9002 U6A740059X	ZN7400E	9002	MC7400P	DM8000N	FJH131	SFC400E	FLH101	N7400A N8480A	US7400A	SN7400N	TG7400E
-	FJH231	- U6A740159X	ZN7401E	-	MC7401P	DM8001N	FJH231	-	FLH201	N7401A N8881A	US7401A	SN7401N	TG7401E
FLH191	FJH221	- U6A740259X	ZN7402E	-	MC7402P	DM8002N	FJH221	SFC402E	FLH191	N7402A -	US7402A	SN7402N	TG7402E
-	-	- U6A740359X	-	-	-	DM8003N	-	-	-	-	US7403A	SN7403N	-
-	-	- U6A740459X	ZN7404E	9016	MC7404P	DM8004N	FJH241	SFC404E	-	-	US7404A	SN7404N	TH7404E
FLH111	FJH121	9003 U6A741059X	ZN7410E	9003	MC7410P	DM8010N	FJH121	SFC410E	FLH111	N7410A N8470A	US7410A	SN7410N	TG7410E
FLH121	FJH111	9004 U6A742059X	ZN7420E	9004	MC7420P	DM8020N	FJH111	SFC420E	FLH121	N7420A -	US7420A	SN7420N	TG7420E
FLH131	FJH101	- U6A743059X	ZN7430E	-	MC7430P	DM8030N	FJH101	SFC430E	FLH131	N7430A N8808A	US7430A	SN7430N	TG7430E
FLH141	FJH141	9009 U6A744059X	ZN7440E	9009	MC7440P	DM8040N	FJH141	SFC440E	FLH141	N7440A N8455A	US7440A	SN7440N	TG7440E
-	FJL101	- U6B744159X	ZN7441E	-	-	DM8840N	-	SFC441E	-	N7441B -	US7441B	SN7441AN	TD7441AE
-	-	-	-	-	-	DM8842N	-	-	-	-	-	SN7442N	-
FLH151	FJH151	9005 U6A745059X	ZN7450E	9005	MC7450P	DM8050N	FJH151	SFC450E	FLH151	N7450A N8840A	US7450A	SN7450N	TG7450E
-	FJH161	- U6A745159X	ZN7451E	-	MC7451P	DM8051N	FJH161	SFC451E	FLH161	N7451A -	US7451A	SN7451N	TG7451E
FLH171	FJH171	- U6A745359X	ZN7453E	-	MC7453P	DM8053N	FJH171	SFC453E	FLH171	N7453A -	US7453A	SN7453N	TG7453E
-	FJH181	- U6A745459X	ZN7454E	-	MC7454P	DM8054N	FJH181	SFC454E	FLH181	N7454A -	US7454A	SN7454N	TG7454E
FLY101	FJY101	9006 U6A746059X	ZN7460E	9006	MC7460P	DM8060N	FJY101	SFC460E	FLY101	N7460A N8806A	US7460A	SN7460N	TG7460E
FLJ111	FJJ111	- U6A747259X	ZN7472E	-	MC7472P	DM8540N	FJJ111	SFC472E	FLJ111	N7472A -	US7472A	SN7472N	TF7472E
FLJ121	FJJ121	- U6A747359X	ZN7473E	-	MC7473P	DM8501N	FJJ121	SFC473E	FLJ121	N7473A -	US7473A	SN7473N	TF7473E
FLJ141	FJJ131	- U6A747459X	ZN7474E	-	MC7474P	DM8510N	FJJ131	SFC474E	FLJ141	N7474A N8828A	US7474A	SN7474N	TF7474E
FLJ151	FJJ181	- U6A747559X	ZN7475E	-	MC7475P	DM8550N	FJJ181	SFC475E	FLJ151	N7475B N8275B	US7475B	SN7475N	TL7475E
FLJ131	FJJ191	- U6A747659X	ZN7476E	-	MC7476P	DM8500N	FJJ191	SFC476E	FLJ131	N7476B -	US7476B	SN7475N	TF7476E
-	-	-	-	-	-	DM8283N	-	-	-	-	US7483B	SN7483N	TA7483E
-	-	-	-	-	-	DM8086N	-	SFC486E	-	-	-	SN7486N	-
FLJ161	FJJ141	- U6A749059X	-	-	-	DM8530N	FJJ141	SFC490E	FLJ161	-	US7490A	SN7490N	TC7490E
-	FJJ251	- U6A749259X	-	-	-	DM8532N	FJJ251	SFC492E	-	-	US7492A	SN7490N	TC7492E
-	FJJ211	- U6A749359X	-	-	MC7493P	DM8533N	FJJ211	SFC493E	-	-	US7493A	SN7493N	TC7493E

PHILIPS

INDICATOR TUBE

ZM1000
ZM1000R

Long life cold cathode ten digit indicator tube for side viewing

QUICK REFERENCE DATA

Numeral height		approx.	14 mm
Numerals		0 1 2 3 4 5 6 7 8 9	
Decimal point		to the left of the numerals	
Supply voltage	V_{ba}	min.	170 V
Anode current, average	I_a		2.5 mA
peak	I_{ap}	max.	12 mA

GENERAL

The numerals are 14 mm high and appear on the same base line allowing in-line read out. The ZM1000R is provided with a red contrast filter.

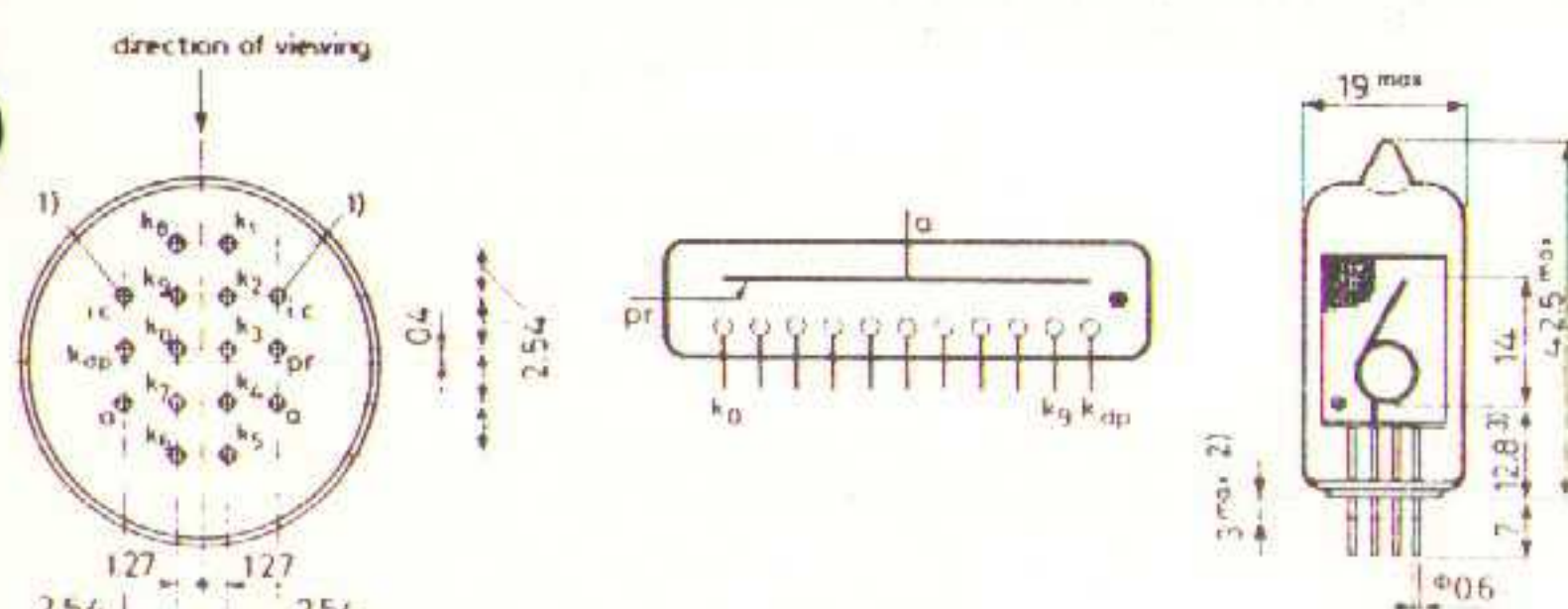
PRINCIPLE OF OPERATION

The tube contains ten cathodes in the form of ten numerals and one in the form of a decimal point; a primer, and one common anode. By applying a suitable voltage between the anode and one of the cathodes the corresponding numeral or the decimal point will be covered by a red neon glow.

The primer allows ionization without delay in strobe type or blanking applications.

DIMENSIONS AND CONNECTIONS

Dimensions in mm



- 1) Length of i.e. pins max. 2.8 mm.
2) Not timed.
3) Standard spread 0.13 mm.

Typical operation over full temperature range 0 °C to +70 °C.

D.C. operation see pages 4, 5, 6 and 7.

Pulse operation

Peak currents up to 12 mA can be allowed provided the average current value does not exceed 2.5 mA.

To avoid excessive glow on "off" cathodes, the cathode selecting voltage should exceed 65 V. Minimum pulse duration 100 µs.

For further information consult the manufacturer.

LIFE EXPECTANCY at $I_a = 2.5$ mA

This tube is manufactured on the same physical principles as other tubes in this category and it is expected that the life will be comparable, viz:

Sequentially changing the display from one digit to the others every 1000 h or less

Mean time between failures min. 200 000 h

LIMITING VALUES (Absolute max. rating system)

Anode voltage necessary for ignition	V_a	min.	170 V
Anode current,			
average during any conduction period	I_a	min.	1.5 mA
average ($T_{av} = 20$ ms)	I_a	max.	4.5 mA
peak	I_{ap}	max.	20 mA
Cathode selecting voltage	V_{kk}	see page 5	
Bias voltage between anode and "off" cathodes	V_{bias}	max.	$V_{floating}$
Ambient temperature	t_{amb}	min.	-50 °C ¹⁾
	t_{amb}	max.	+70 °C

¹⁾ Bulb temperatures below 10 °C result in a reduced life expectancy and changes in characteristics (see page 4).

For equipment to be used over a wide temperature range, "constant current operation" (high supply voltage with a high anode series resistor) is recommended.

The deviations of the axis of the pins with respect to the true geometrical position cover an area of max. 0.3 mm diameter. The pin configuration is compatible with the reference grid for printed wiring according to IEC Publication 97 (0.1 in).

Mounting position: Any

Soldering

The pins may be dip-soldered at a solder temperature of max. 240 °C for maximum 10 seconds up to a point 5 mm from the seals.

Natural frequency

The natural frequencies of the numeral cathodes lie within the range from 300 Hz to 800 Hz.

ACCESSORIES

55701 Printed wiring mounting board (19 x 100 mm) on which the ZM1000 can be soldered; afterwards the combination can be mounted on a vertical printed wiring board carrying, e.g., the drive circuit. Can also be used with the snap-fit tube holder 55703.

55702 Tube socket (for 0.1 in grid). Phenolic. Tinned contacts.

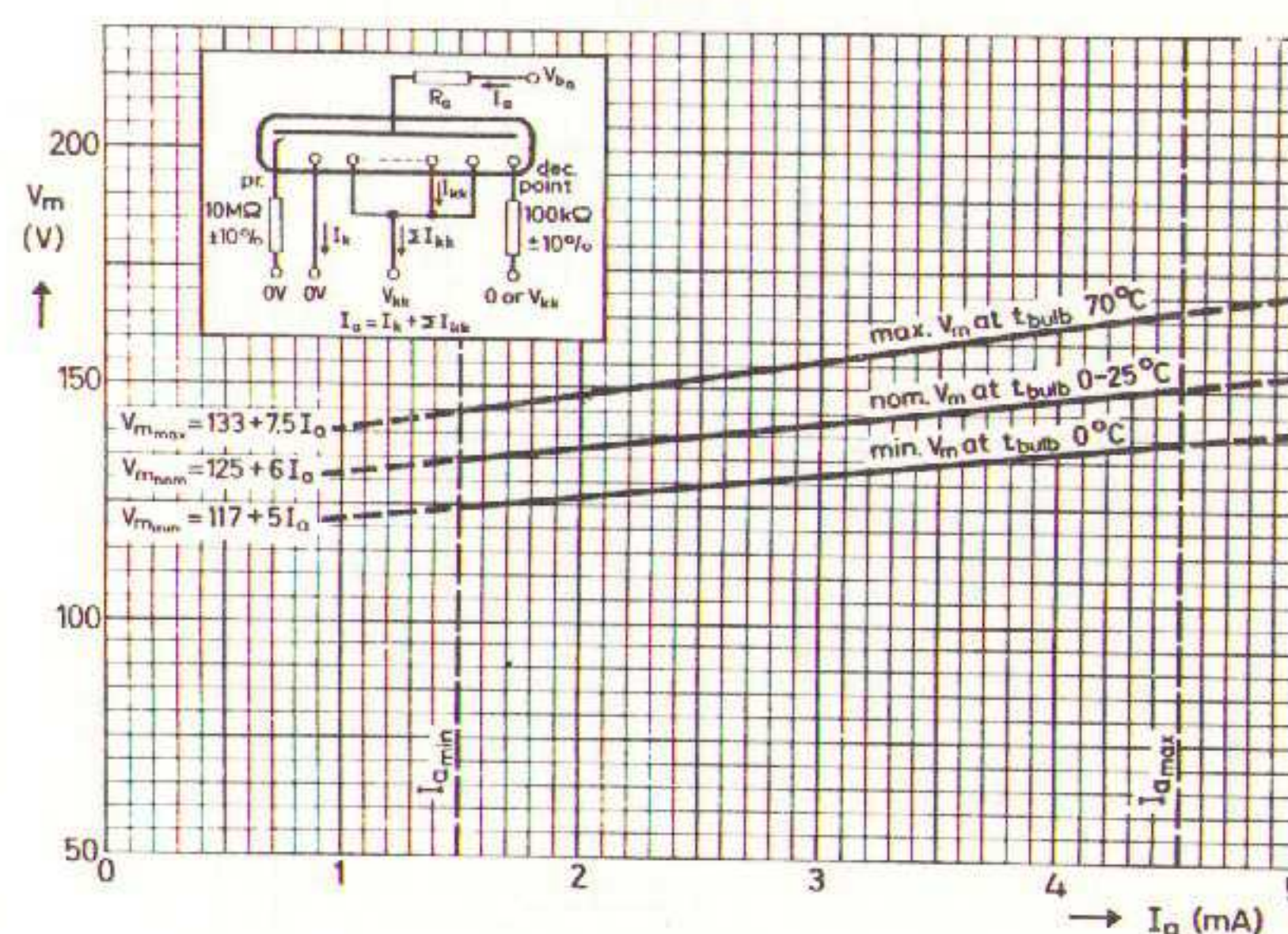
55703 Snap-fit tube holder.

55704 Set of one left-hand and one right-hand end piece to complete the snap-fit indicator tube assembly.

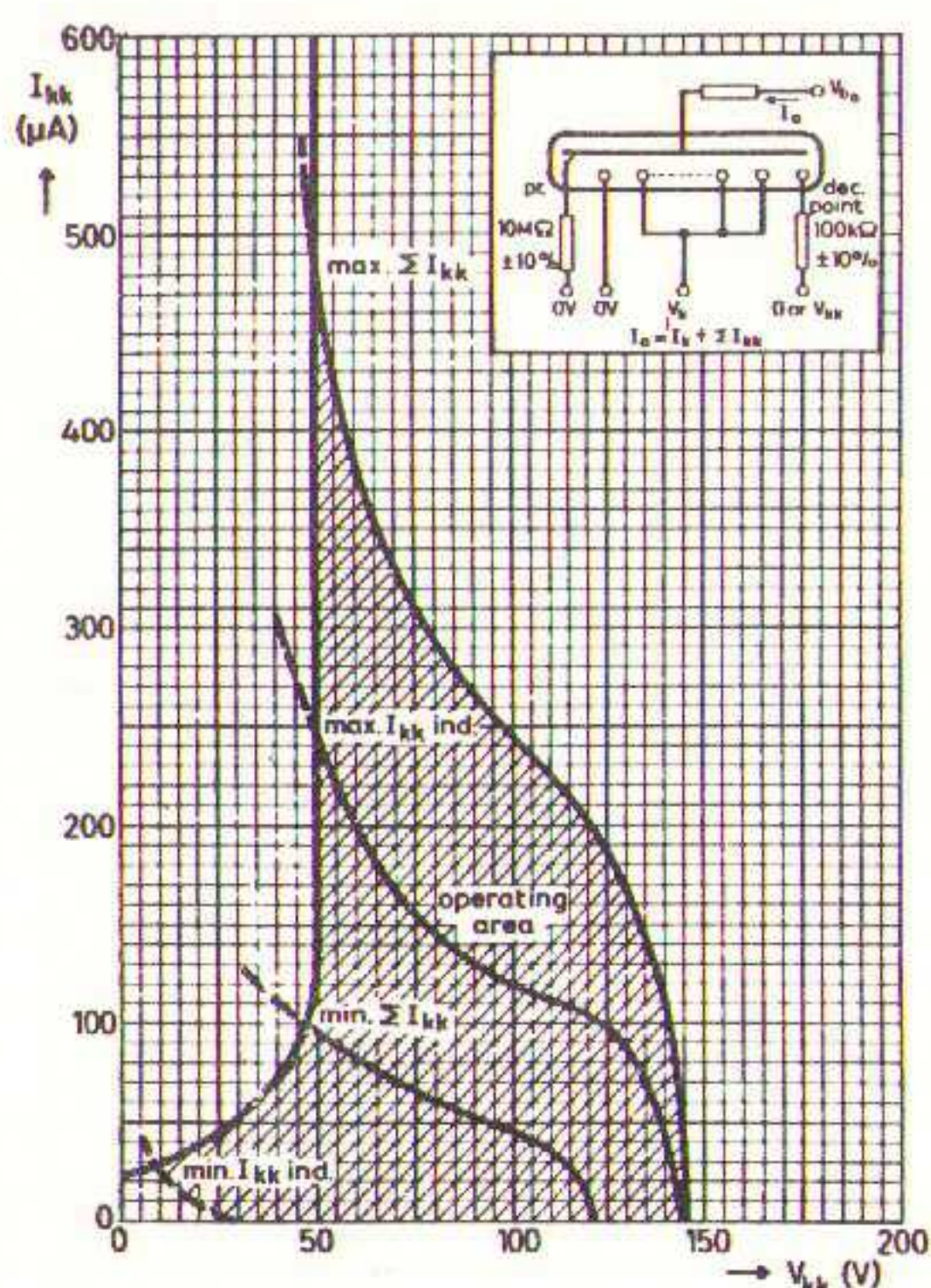
CHARACTERISTICS AND OPERATING CONDITIONS

Ignition voltage	V_{ign}	max.	170 V
Maintaining voltage	V_m	see page 4	
Anode current for coverage	I_a	min.	1.5 mA
(with or without decimal point and	I_a	max.	4.5 mA
$V_{kk} = V_{kk_{min}} - V_{fl}$, see page 5)			
Cathode selecting voltage	V_{kk}	see page 5	
Cathode resistor, decimal point	R_{dp}	100 kΩ ± 10% ¹⁾	
Primer resistor	R_{pr}	10 MΩ ± 10%	
Extinction voltage	V_{ext}	min.	118 V

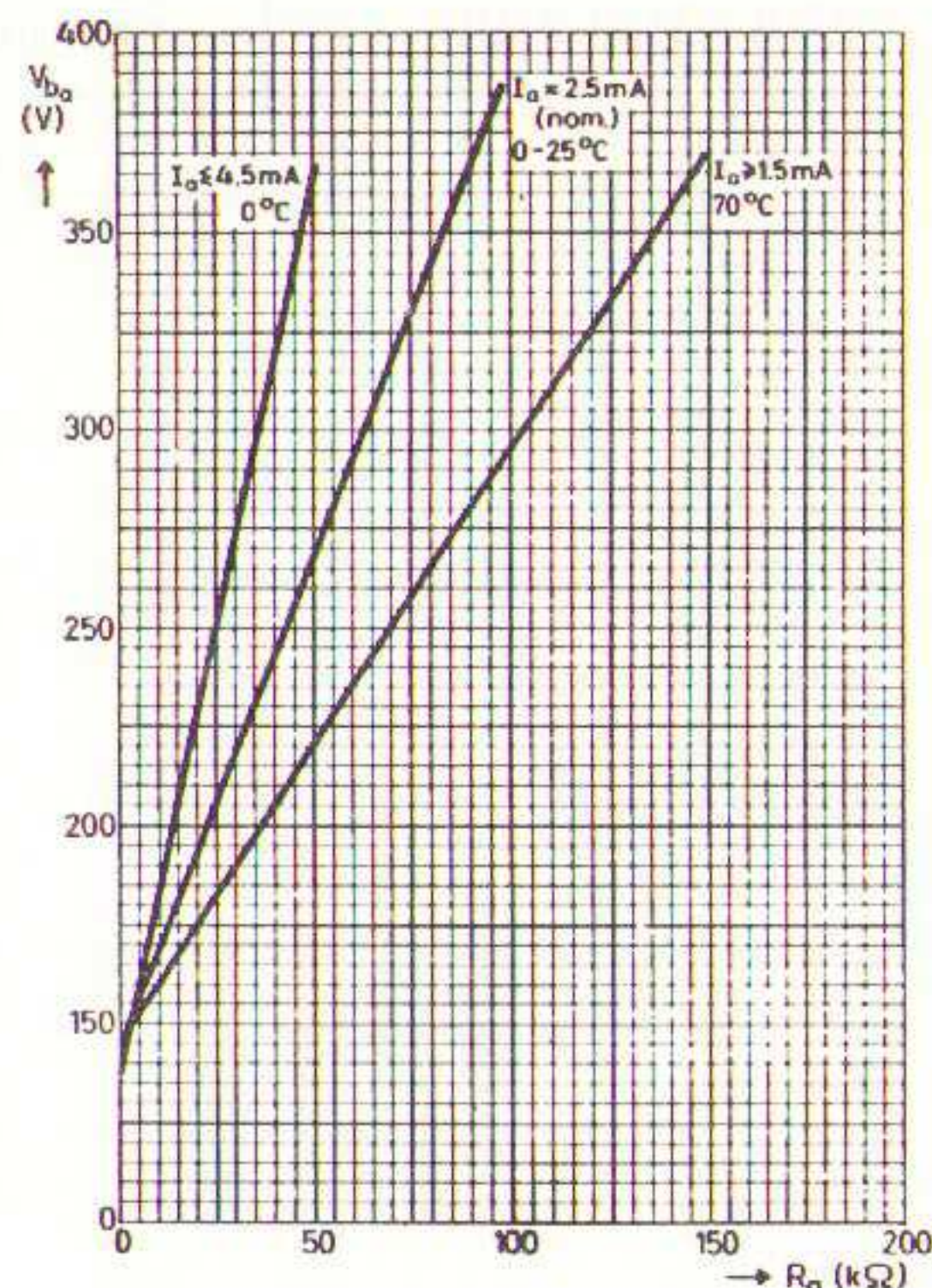
¹⁾ Lower values of this resistor are permitted. The anode current should be increased by the increase of decimal point current resulting from the decrease of this resistor.



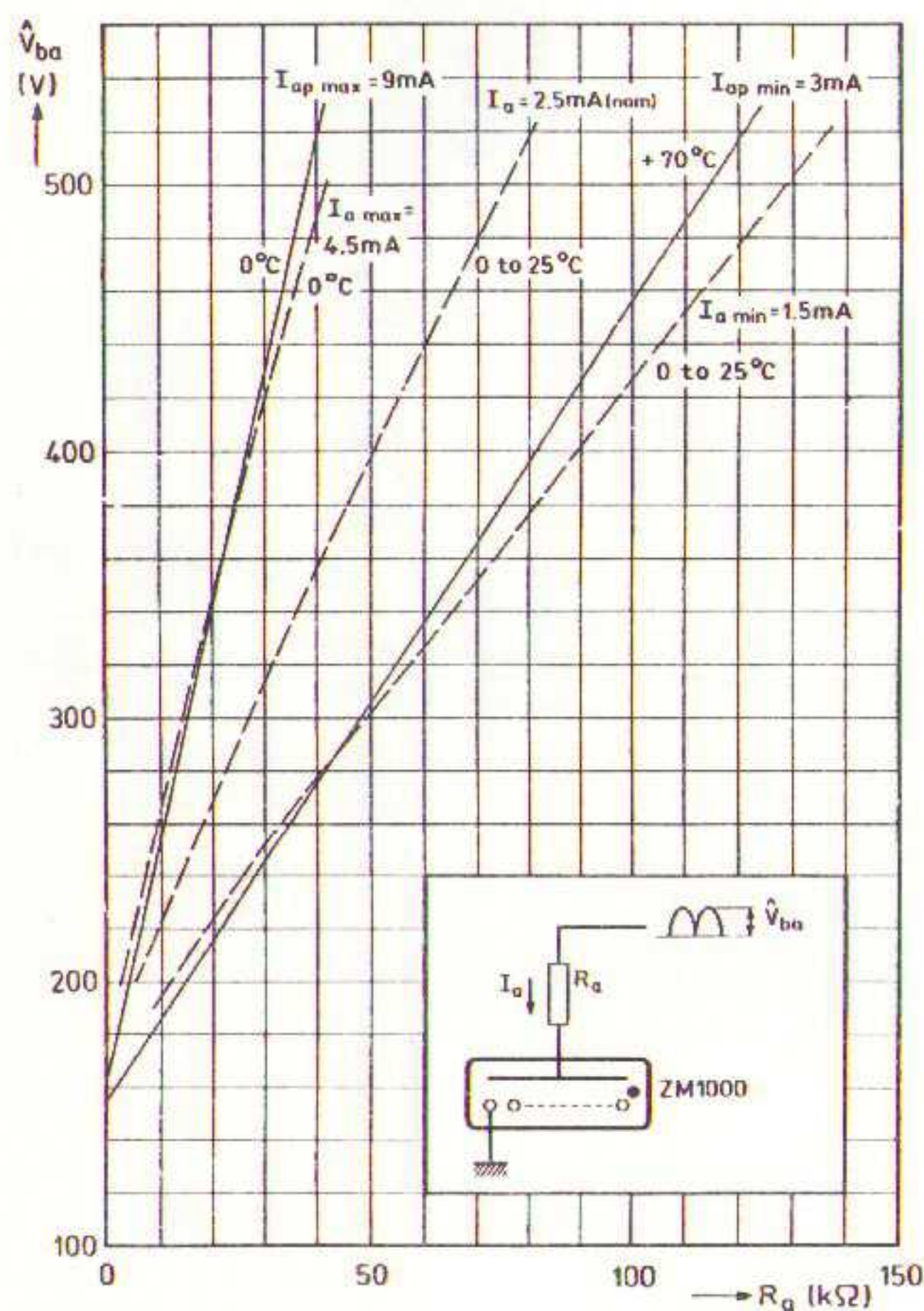
ZM1000 ZM1000R



I_{kk} individual and ΣI_{kk} versus cathode selecting voltage V_{kk} at $I_a = 2.5 \text{ mA}$.
 I_{kk} and ΣI_{kk} are proportional to the anode current within the operating range of I_a and with $V_{kk} = 0 \text{ V}$ to 100 V .
 The curves are valid for instantaneous values and for average values of anode current.



Graph denoting the relationships of D.C. anode supply voltage and required anode resistor to remain within the recommended operating region.



Op pagina 69, 70, 71, 72 en 73 hebben wij de datasheets opgenomen van verscheidene koude kathode indicatie buizen van o.a. Philips en STC. Deze buizen lenen zich voor toepassingen, waarbij de levensduur van minimaal 100.000 uur voldoende is en een hoogspanning van 170 tot 250 volt ter beschikking staat. Denken we aan een werkelijk portable gebruik van een elektronisch telsysteem, dan zou aan het geheel een omvormer moeten worden toegevoegd voor opwekking van de anode-spanning; gezien de stroomafname behoeft dit niet altijd een bezwaar te zijn.

Langs deze weg wijzen wij echter op een nieuw soort cijferindicator van o.a. Mosanto. Deze indicator is opgebouwd uit licht uitstralende dioden (LED's) en in zeven-segment configuratie aangebracht in een kleine behuizing. Door de eigenschappen van een LED is het mogelijk uit een zevensegment decoder/buffer versterker deze indicator te sturen, waarbij een goede duidelijkheid en afleesbaarheid wordt verkregen door de grote lichtopbrengst van de LED's.

In deze documentatie zullen we echter de verdere bespreking van dit device nog even achterwege laten, aangezien op dit moment o.i. alleen gebruik op grotere schaal financieel is verantwoord (stuksprijs circa f 50,-). Mocht in de toekomst een grote belangstelling ontstaan door een verlaging van de kostprijs, dan zullen wij gaarne uitgebreid op de eigenschappen en het gebruik van deze indicator terugkomen.

voim olom
ELEKTRONICA

HET BEDRIJF, WAAR DE TECHNISCHE
ONTWIKKELINGEN BLIJVEN DOORGAAN

PHILIPS

INDICATOR TUBE

ZM1020

Long life cold cathode ten digit numeral indicator tube for top viewing.

QUICK REFERENCE DATA

Numeral height	15 mm
Numerals	1 2 3 4 5 6 7 8 9 0
Supply voltage	min. 170 V
Anode current	2 mA

GENERAL

The numerals are 15 mm high and appear on the same base line allowing in-line read out. The ZM1020 is provided with a red contrast filter.

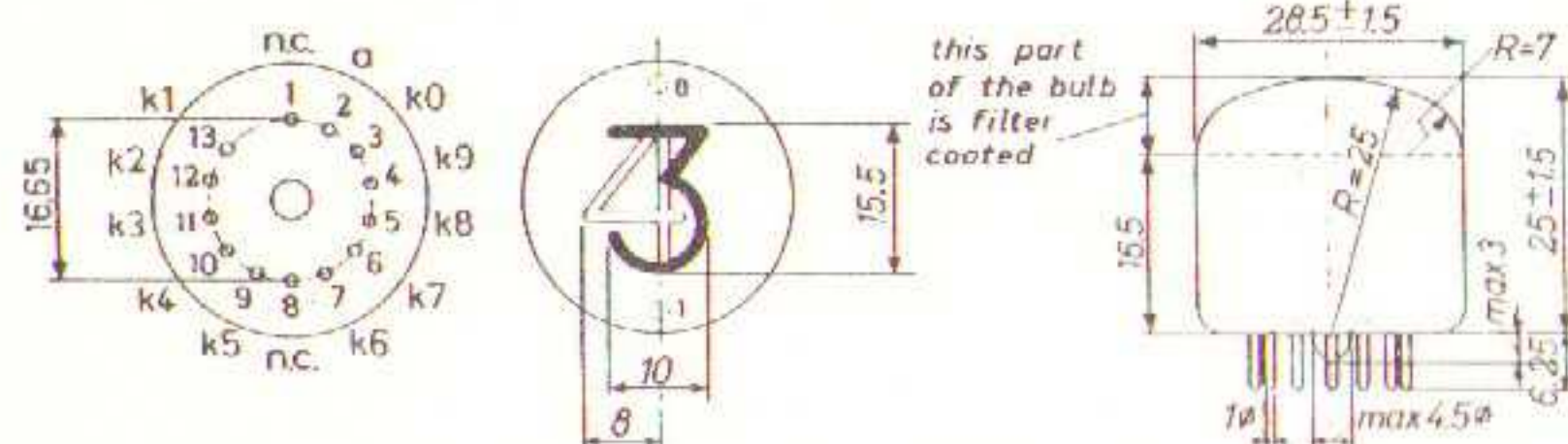
PRINCIPLE OF OPERATION

The tube contains ten cathodes in the form of ten figures and one common anode. By applying a suitable voltage between the anode and one of the ten cathodes the corresponding numeral will be covered by a red neon glow.

DIMENSIONS AND CONNECTIONS

Dimensions in mm

Base: B13B



Mounting position: any

The numerals are viewed through the dome of the envelope. The numerals will appear upright (within 1.5°) when the tube is mounted with the line through pins 1 and 8 vertical, pin 8 being uppermost.

Accessories

Socket type 2422 505 00001
or
2422 505 00002

CHARACTERISTICS AND OPERATING CONDITIONS

(Valid over life and full temperature range)

Ignition voltage	V_{ign}	max. 170 V
Maintaining voltage	V_m	see sheet 4
Anode current for coverage,		
average during any conduction period	I_a	min. 1 mA
Anode current,		
average ($T_{av} = \text{max. } 20 \text{ ms}$)	I_a	max. 3 mA
peak	I_{ap}	max. 6 mA
Cathode selecting voltage	V_{kk}	see sheet 5
Extinguishing voltage	V_{ext}	min. 118 V

Typical operation ¹⁾

D.C. operation

See sheets 5 and 6

A.C. operation

See sheets 5 and 7

¹⁾ Bulb temperatures below 10°C result in a reduced life expectancy and changes in characteristics (see sheet 4). In designing equipment to be used over a wide temperature range the use of "constant current operation" (high supply voltage with a high anode series resistor) is recommended.

LIFE EXPECTANCY AND RELIABILITY (at $I_a = 2 \text{ mA}$)

Sequentially changing the display from one digit to the others every 1000 h, or less

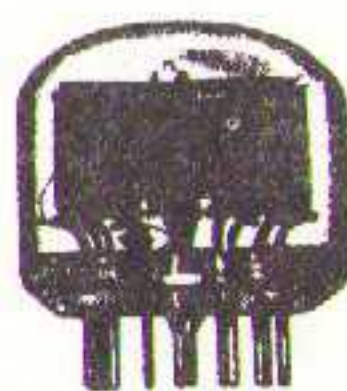
100,000 h

The reliability has been assessed in a life test programme totalling 4.5×10^6 tube hours. The longest test period was 50,000 hrs on 47 tubes. No failures have been found. The Mean Time between Failures is better than 10^6 hrs which corresponds with a failure rate of less than 0.1 % per 1000 hrs at a confidence level of 95 %.

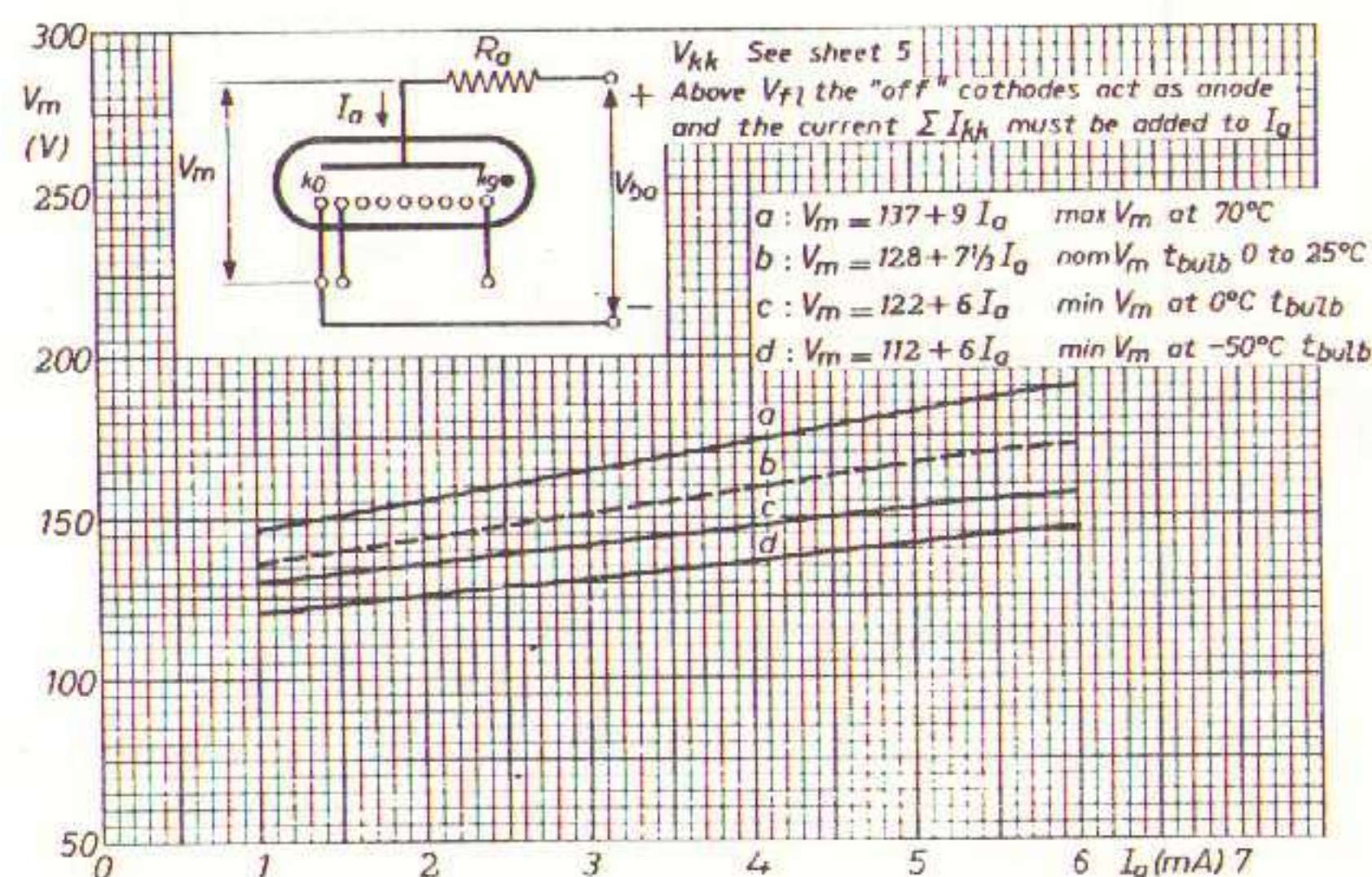
LIMITING VALUES (Absolute max. rating system)

Anode voltage necessary for ignition	V_a	min. 170 V
Anode current, D.C.	I_a	min. 1 mA
rectified A.C. and pulse	I_{ap}	min. 2 mA
average ($T_{av} = \text{max. } 20 \text{ ms}$)	I_a	max. 3 mA
peak	I_{ap}	max. 10 mA ¹⁾
Cathode selecting voltage	V_{kk}	see lines N and W on sheet 5
Bias voltage between anode and "off" cathodes (see sheet 5)	V_{bias}	max. $V_{floating}$
Ambient temperature	t_{amb}	min. -50°C max. $+70^\circ\text{C}$

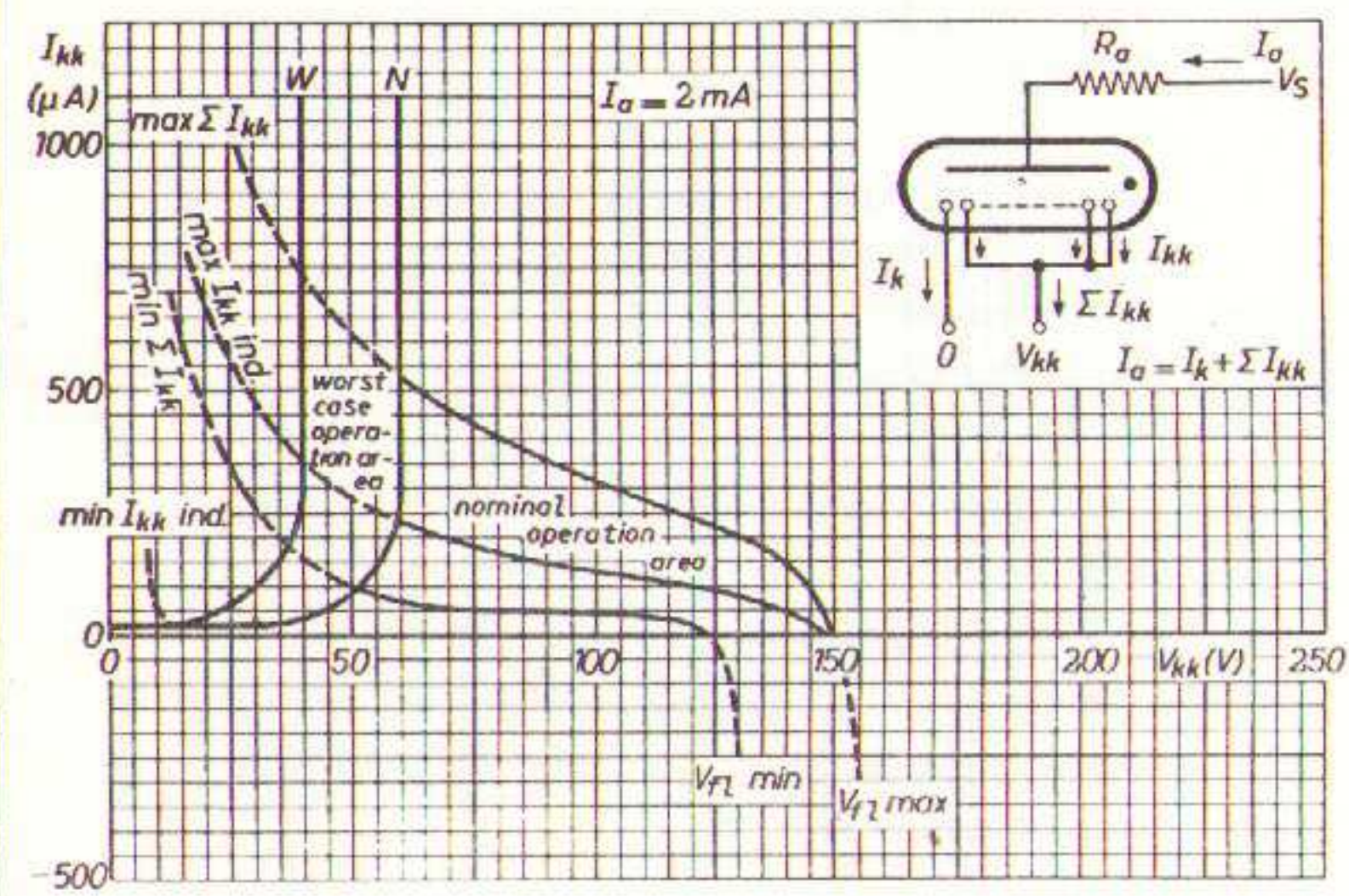
¹⁾ Above $I_a = 6 \text{ mA}$ the connecting wires and eyelets may be covered by the glow.



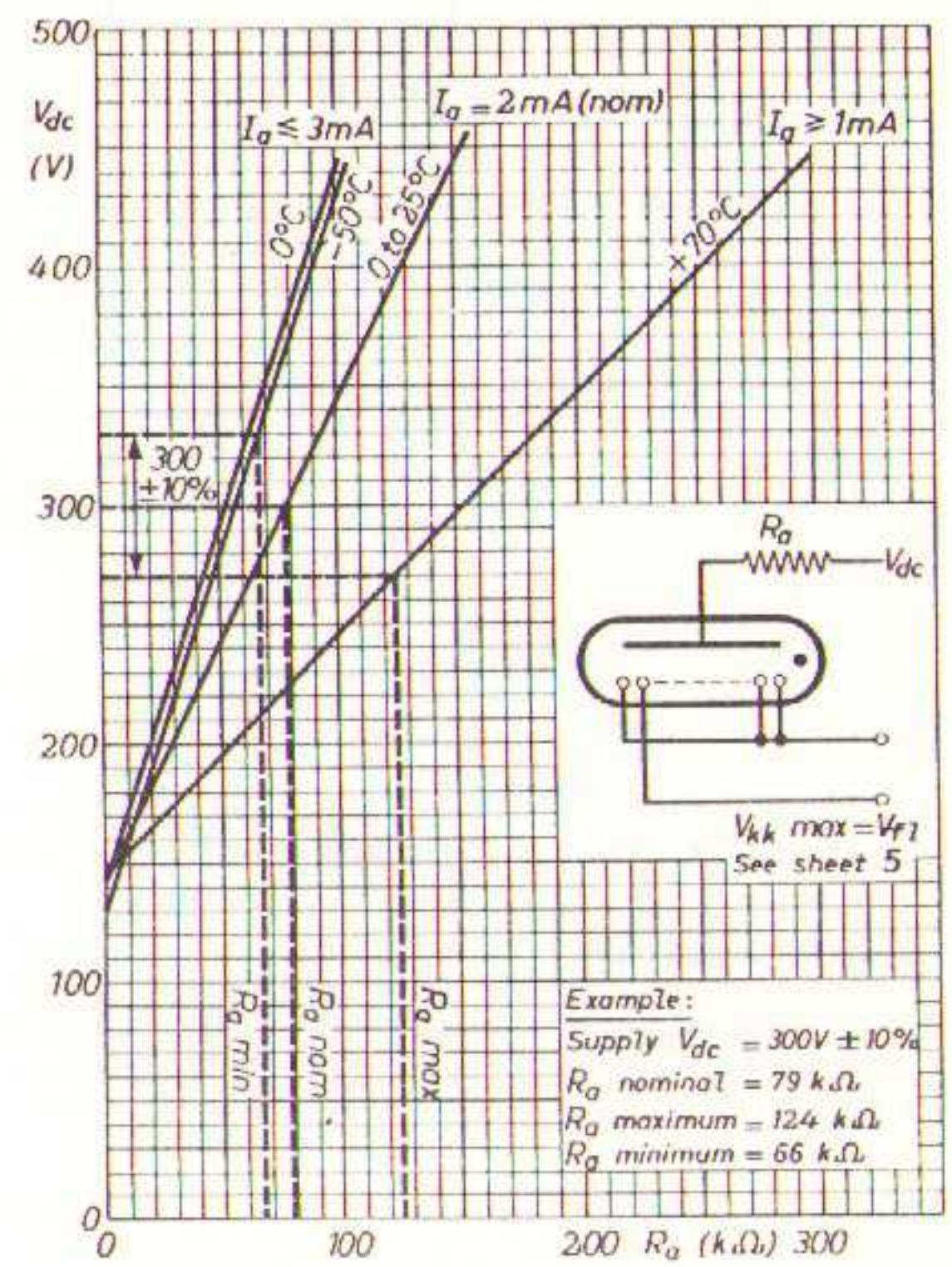
ZM 1020



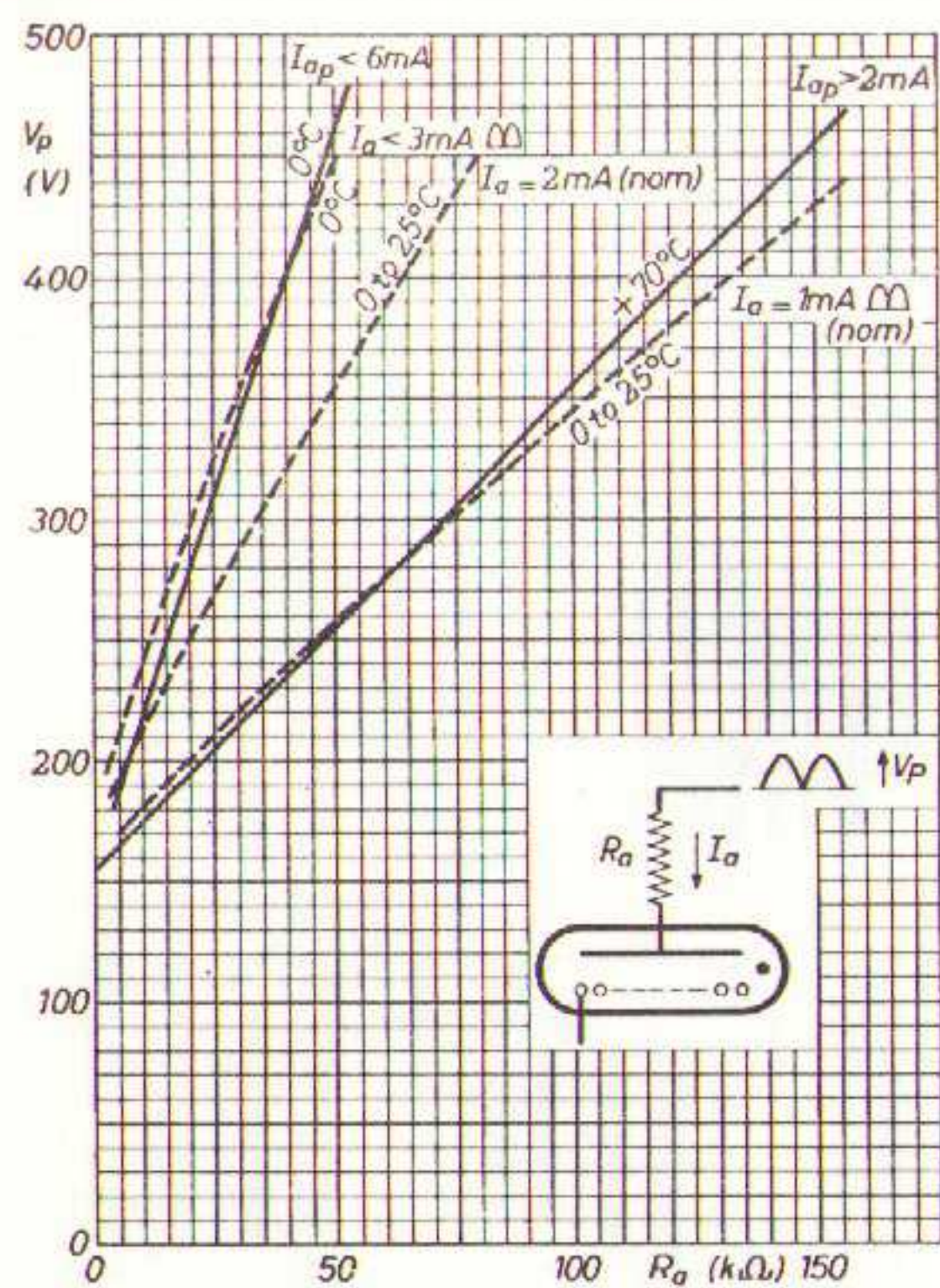
I_{kk} individual and ΣI_{kk} versus cathode selecting voltage V_{kk} at $I_a = 2 \text{ mA}$.
 I_{kk} and ΣI_{kk} are proportional to anode current in the range $V_{kk} = 0$ to 100 V .
 The range of V_{f1} ($I_{kk} = 0$) shifts to the right/left at increasing/decreasing anode current (8 V/mA).
 The curves are valid for instantaneous and for average values of anode current.



For low cathode selecting voltages the current I_{kk} to the "off" cathodes will increase and the readability of the "on" cathode will be affected. It is therefore recommended to use a nominal operating point to the right of line N. Under the worst operating conditions the operating point should never reach the area left of line W.



Graph denoting the relationship of D.C. anode supply voltage and required anode resistor to remain within the recommended operating region.



Graph denoting the relationship of the peak value of full-wave unsmoothed rectified A.C. anode supply voltage and the required anode resistor to remain within the recommended operating area.

PHILIPS

INDICATOR TUBE

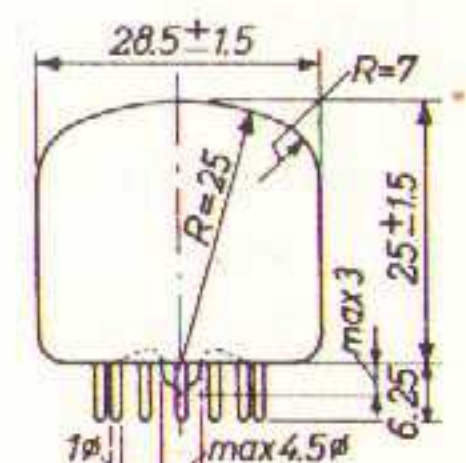
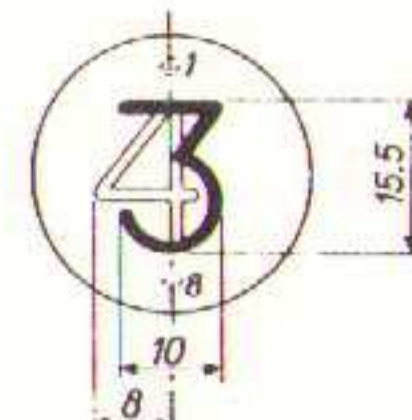
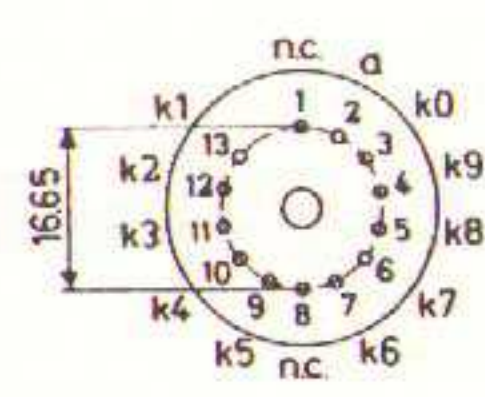
ZM1022

The type ZM1022 is electrically identical with type ZM1020 but has no filter coating.
 The use of a separate blue absorbing e.g. circular polarized amber filter is recommended.

DIMENSIONS AND CONNECTIONS

Dimensions in mm

Base: B13B



STC

INDICATOR TUBE

GN 4 P

Long life cold cathode ten digit numeral indicator for top viewing.

The STC GN4P is electrically identical with type ZM1020 but has a decimal point to the left of the numerals (connection point 8). For the use of this decimal point see also the ZM1000 datasheet. The numeral connections are identical with the type ZM1020 or the type ZM1022.



PHILIPS	INDICATOR TUBE	ZM1021										
Cold cathode character indicator tube for top viewing.												
<table border="1"> <thead> <tr> <th colspan="2">QUICK REFERENCE DATA</th> </tr> </thead> <tbody> <tr> <td>Character height</td> <td>15 mm</td> </tr> <tr> <td>Characters</td> <td>A, V, Ω, $\%$, $\sim$, +, -</td> </tr> <tr> <td>Supply voltage</td> <td>min. 170 V</td> </tr> <tr> <td>Anode current</td> <td>2 mA</td> </tr> </tbody> </table>			QUICK REFERENCE DATA		Character height	15 mm	Characters	A, V, Ω , $\%$, $\sim$, +, -	Supply voltage	min. 170 V	Anode current	2 mA
QUICK REFERENCE DATA												
Character height	15 mm											
Characters	A, V, Ω , $\%$, $\sim$, +, -											
Supply voltage	min. 170 V											
Anode current	2 mA											
DIMENSIONS AND CONNECTIONS Dimensions in mm Base: B13B												
CHARACTERISTICS, OPERATING CONDITIONS AND LIMITING VALUES These are essential the same as of type ZM1020.												

PHILIPS	INDICATOR TUBE	ZM1024				
Cold cathode character indicator tube for top viewing						
<table border="1"> <thead> <tr> <th colspan="2">QUICK REFERENCE DATA</th> </tr> </thead> <tbody> <tr> <td>Characters</td> <td>c/s, Kc/s, Mc/s, μs, ms, ns, s</td> </tr> </tbody> </table>			QUICK REFERENCE DATA		Characters	c/s, Kc/s, Mc/s, μ s, ms, ns, s
QUICK REFERENCE DATA						
Characters	c/s, Kc/s, Mc/s, μ s, ms, ns, s					
This tube is mechanically compatible with type ZM1020						
DIMENSIONS AND CONNECTIONS Dimensions in mm Base: B13B						
CHARACTERISTICS, OPERATING CONDITIONS AND LIMITING VALUES These are essential the same as of type ZM1020.						

Naast de in deze documentatie besproken produkten treft U in ons voorraad-programma ook vele produkten aan, welke in combinatie hiermee uitstekend gebruikt kunnen worden. Voor een gedeelte hiervan verwijzen wij naar onze prijslijst "digitale produkten". Wij noemen U hieruit:

PRINTVOETEN voor 14 en 16 pens dual-in-line IC's. Deze voeten zijn uitgevoerd met vergulde contacten met een overgangswaerstand van maximaal 0,005 Ω . De minimum isolatiewaerstand bedraagt $4 \times 10^{14} \Omega$, terwijl de maximale belastingsstroom per contact 1 amp. mag bedragen. Wij wijzen erop, dat deze uitvoering printvoet (van het fabriekat Barnes) zich door zijn geringe bouwhoogte, hoogwaardige contactkwaliteit en geringe prijs uitstekend leent voor permanent gebruik in digitale systemen.

DUIMWIJLSCHAKELAARS kunnen in vele systemen worden toegepast, waarbij een bepaalde functie, welke instelbaar dient te zijn, moet worden onttrokken of worden toegevoegd aan het logische systeem. We kunnen hierbij o.a. denken aan een teller met voorkeuze instelling (en wat dacht U van een decade-bank??). Deze duimwijschakelaars kunnen in verscheidene uitvoeringen en afmetingen geleverd worden met zowel decimale als binaire code. Voor nadere gegevens kunt U contact opnemen met onze afdeling verkoop.

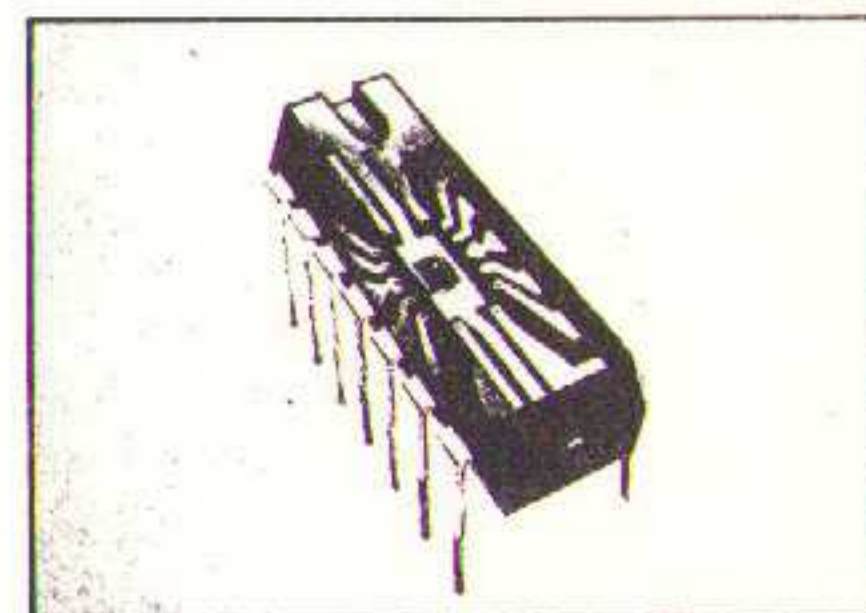
TAPEMATERIALEN zijn bij het vervaardigen van printen in digitale systemen onontbeerlijk. Door de vergaande miniaturisatie, welke ook in de bedrading tussen de diverse IC's tot uiting komt, is het vervaardigen van printen langs fotografische weg een noodzaak geworden. Daartoe levert Van Dam Elektronica U ook etssets volgens het foto-positief procédé (!!!), bestaande uit fotoresist, ontwikkelaar, reinigingsmiddel en etsmiddel; hiervoor is ook pertinax of glasvezel printplaat leverbaar, 0,1' transparant rastermateriaal, tapes en cirkels voor het vervaardigen van printtekeningen e.d. Zie voor deze produkten ook onze prijslijst "digitale produkten".

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heeft niet alles, alleen het beste.

plastic dual-in-line

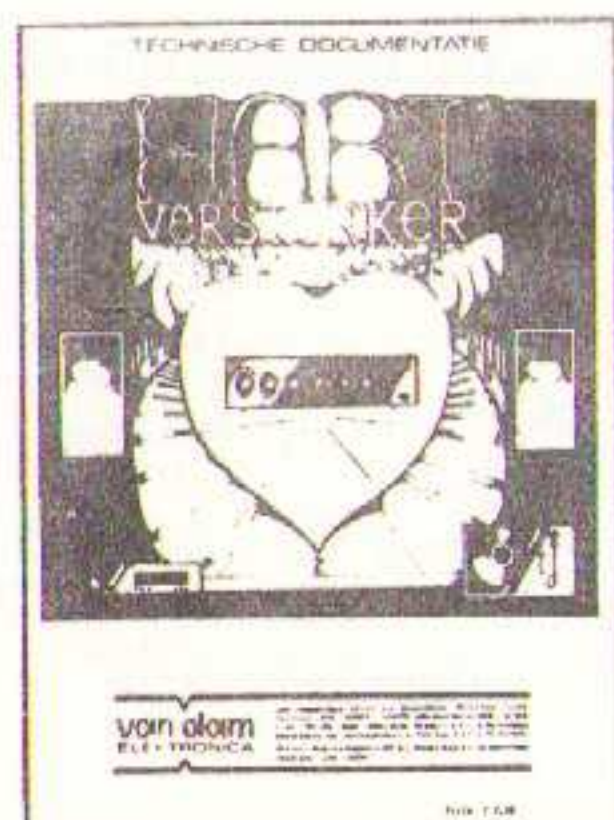
TI's plastic dual-in-line packages are rugged and low in cost. They are backed by millions of device-hours of reliability data.



14-PIN PLASTIC DUAL-IN-LINE N-PACKAGE OUTLINE	
	NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins (4) and (11). b. All dimensions are in inches unless otherwise noted. c. This dimension does not apply for solder-dipped leads. d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.
Falls Within TO-116 Dimensions	
16-PIN PLASTIC DUAL-IN-LINE N-PACKAGE OUTLINE	
	NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins (1) and (16). b. All dimensions are in inches unless otherwise noted. c. This dimension does not apply for solder-dipped leads. d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.
Falls Within TO-116 Dimensions	

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Technische Documentatie 1970, deel 1-4, behandelde in zijn geheel de technische gegevens, ontwikkelachtergrond, beschermmogelijkheden, testrapporten, testapparaat, frequentie-compensatie en vele toepassingen van de operationele versterker 709. Wilt U hiervan meerdere exemplaten hebben, dan kan deze documentatie ook los worden aangeschaft door storting van f 5,20 op onze postgirorekening 295550 t.n.v. Van Dam Elektronica n.v., Rotterdam-noord, Holland, onder vermelding van: t.b.v. Technische Documentatie 1970 DEEL 1 t/m 4.



Op dezelfde wijze kunt U ook in het bezit komen van de tweede en herziene druk van de documentatie/bouwbeschrijving van de zo bekend geworden "HART"-versterker. Deze versterker, welke onder de bouwpakketten nog geen tegenhanger heeft, is ook in november 1969 door de redactie van Radio Bulletin getest en besproken. De prijs van deze documentatie bedraagt f 2,50.

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GIRO 295550

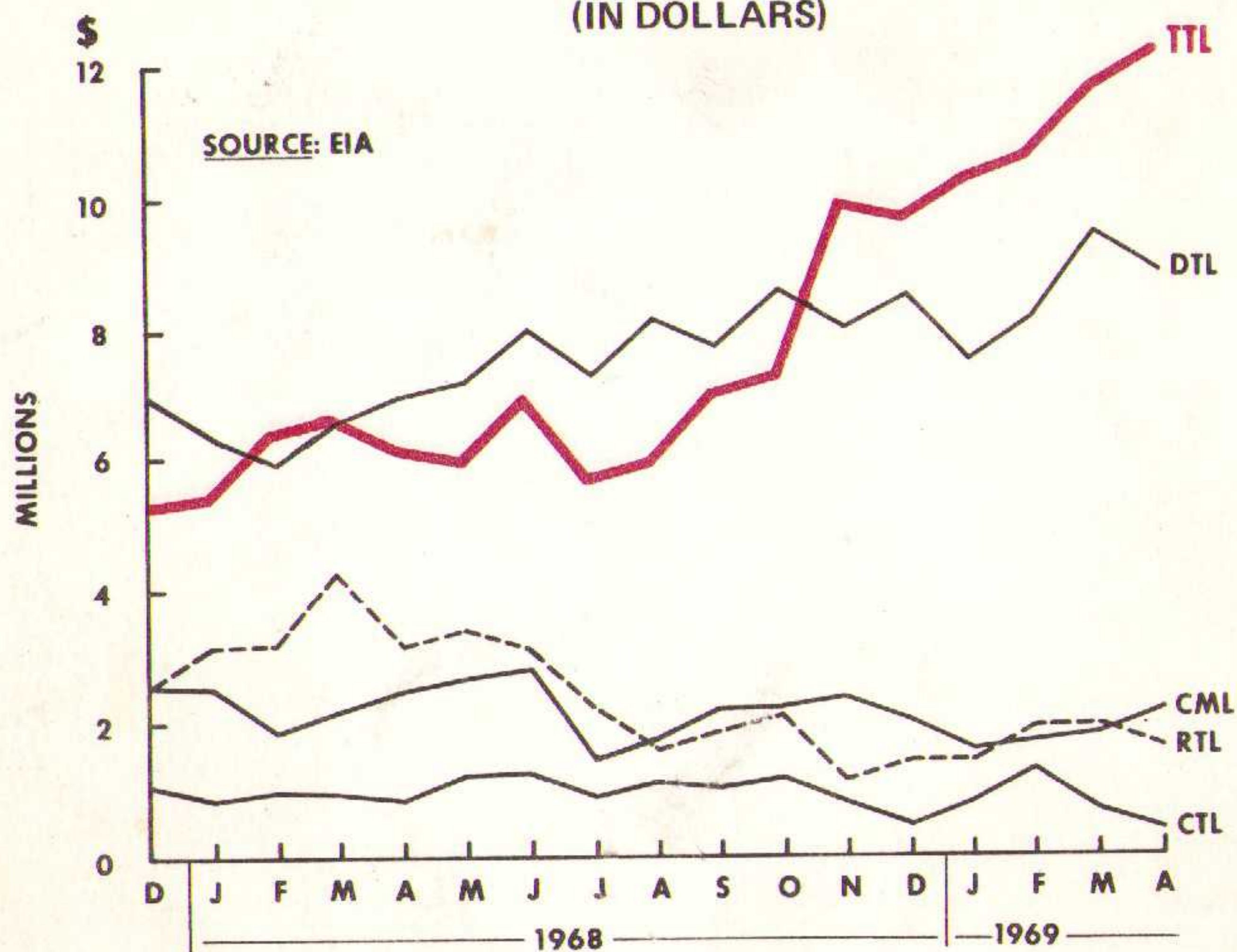
Naast deze technische gegevens kunt U regelmatig in de vakliteratuur toepassingen en nadere beschrijvingen van TTL geïntegreerde schakelingen aantreffen. Wij houden met opzet het verdere gedeelte van deze pagina open, teneinde U in de gelegenheid te stellen, hierop de artikelen, welke U interessant vond en eventueel wilt kunnen naslaan, te noteren.

[illegible]

..... de tendens is TTL; zie pag. 76.

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